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VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ

FACULTY OF MECHANICAL ENGINEERING
FAKULTA STROJNÍHO INŽENÝRSTVÍ

INSTITUTE OF PHYSICAL ENGINEERING
ÚSTAV FYZIKÁLNÍHO INŽENÝRSTVÍ

PREPARATION OF LOW-DIMENSIONAL III-V SEMICONDUCTORS
PŘÍPRAVA NÍZKODIMENZIONÁLNÍCH III-V POLOVODIČŮ

MASTER'S THESIS
DIPLOMOVÁ PRÁCE

AUTHOR — **Bc. Silvestr Stanislav**
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SUPERVISOR — **doc. Ing. Miroslav Kolíbal, Ph.D.**
VEDOUCÍ PRÁCE

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BRNO UNIVERSITY OF TECHNOLOGY
FACULTY OF MECHANICAL ENGINEERING

Assignment Master's Thesis

Institut:	Institute of Physical Engineering
Student:	**Bc. Silvestr Stanislav**
Degree programm:	Physical Engineering and Nanotechnology
Branch:	no specialisation
Supervisor:	**doc. Ing. Miroslav Kolíbal, Ph.D.**
Academic year:	2020/21

As provided for by the Act No. 111/98 Coll. on higher education institutions and the BUT Study and Examination Regulations, the director of the Institute hereby assigns the following topic of Master's Thesis:

Preparation of low–dimensional III–V semiconductors

Brief Description:

The group of surfaces and nanostructures at UFI operates a dedicated vacuum chamber for deposition of III–V semiconductors (III – arsenides, antimonides). These materials are a subject of intensive research and are already commercionalized. The student will learn how to operate this vacuum system and will plan & prepare low–dimensional (quantum dots, nanowires) semiconductors with specific properties (e.g. photoluminescence).

Master's Thesis goals:

1. Learn how to operate MBE chamber.
2. Prepare suitable catalysts for III–V semiconductor growth.
3. Prepare Ga, In(As, Sb) nanostructures.

Recommended bibliography:

GAO, Qian, Vladimir G DUBROVSKII, Philippe CAROFF, et al. Simultaneous Selective-Area and Vapor-Liquid-Solid Growth of InP Nanowire Arrays. Nano letters [online]. 2016, 16(7), 4361-4367 [cit. 2020-10-19]. ISSN 15306984. Dostupné z: doi:10.1021/acs.nanolett.6b01461

VUKAJLOVIC-PLESTINA, J, W KIM, L GHISALBERTI, et al. Fundamental aspects to localize self-catalyzed III-V nanowires on silicon. Nature Communications [online]. London: Nature Publishing Group, 2019, 10(1) [cit. 2020-10-19]. Dostupné z: doi:10.1038/s41467-019-08807-9

Deadline for submission Master's Thesis is given by the Schedule of the Academic year 2020/21

In Brno,

L. S.

prof. RNDr. Tomáš Šikola, CSc. Director of the Institute	doc. Ing. Jaroslav Katolický, Ph.D. FME dean

ABSTRACT

The diploma thesis deals with the preparation of nanostructures from indium arsenide (InAs) using the molecular beam epitaxy (MBE) method. Emphasis is placed on the production of structures in the form of nanowires on a silicon substrate. The introductory part of the thesis describes the motivation for the study of III-V semiconductors and specifically InAs. The following chapters explain two basic principles of nanowire formation. The experimental part of the work discusses the possibility of preparing an indium catalyst for self-seeded InAs nanowire growth in a specific MBE apparatus. The following part presents the results of InAs nanowires growth via the selective area epitaxy (SAE) mechanism. The nanowires were fabricated on a substrate with thermally decomposed silicon dioxide and on a substrate with a lithographically prepared silicon dioxide mask.

ABSTRAKT

Tato diplomová práce se zabývá přípravou nanostruktur z indium arsenidu (InAs) pomocí metody molekulární svazkové epitaxe (MBE). Důraz je kladen na výrobu struktur ve formě nanodrátů na křemíkovém substrátu. V úvodní části práce je popsána motivace pro studium III-V polovodičů a konkrétně InAs. Následující kapitoly vysvětlují dva základní princpy tvorby nanodrátů. Experimentální část práce diskutuje možnost přípravy indiového katalyzátoru pro samokatalyzovaný růst InAs nanodrátů v konkrétní aparatuře MBE. Následuje prezentace výsledků růstu InAs nanodrátů mechanismem selektivní epitaxe (SAE). Nanodráty byly vyrobeny na substrátu s termálně dekomponovaným oxidem a rovněž na substrátech s litograficky připravenou oxidovou maskou.

KEYWORDS

nanowires, indium arsenide, InAs, selective area epitaxy, SAE, vapour-liquid-solid growth, VLS, molecular beam epitaxy, MBE, catalytic nanoparticles

KLÍČOVÁ SLOVA

nanodráty, arsenid inditý, InAs, selektivní epitaxe, SAE, vapour-liquid-solid růst, VLS, molekulární svazková epitaxe, MBE, katalytické nanočástice

STANISLAV, S. Preparation of low-dimensional III-V semiconductors: Master's thesis. Brno: Brno University of Technology, Faculty of Mechanical Engineering, Institute of Physical Engineering, 2021. 52 p. Supervised by doc. Ing. Miroslav Kolíbal, Ph.D.

I hereby declare that this thesis is my original work, written under the guidance of the thesis supervisor doc. Ing. Miroslav Kolíbal, Ph.D. I also declare that all the information obtained from technical literature and other sources is properly cited and all the sources are listed at the end of the thesis.

Bc. Silvestr Stanislav

I hereby thank my supervisor doc. Ing. Miroslav Kolíbal, Ph.D., for his guidance throughout the thesis, for his enthusiasm and ability to always motivate me. I wish to express my thanks to Ing. Tomáš Musálek for sharing his deep knowledge about MBE and for valuable advice concerning experiments. I also wish to express my thanks to people who helped me with some experimental techniques, namely, Ing. Daniel Citterberg for introducing me to electron beam lithography, Mgr. Peter Kepič for his help with ellipsometry, Ing. Martin Kovařík for help with AFM and XPS measurements. My great thanks go to my awesome classmates who made the studies an unforgettable experience and without whom it would not be as enjoyable and funny. I wish to extend my special thanks to Karel Vařeka, for providing the FIB experiments, although they are not listed in the thesis and for numerous table tennis battles. I wish to extend my special thanks to Daniel Šimek for our endless discussions and for his moral support when times seemed to be hard. Last but not least I would like to thank to my parents from the bottom of my heart for they support throughout my entire life.

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Bc. Silvestr Stanislav

CONTENTS

1 INTRODUCTION

Semiconductor materials have played and continue to play an irreplaceable role in technology, and their development has literally changed the way human civilization works. Over time, the semiconductor industry has become one of the technological pillars of modern civilization. Silicon has been a key element in the semiconductor industry since the beginning of scientific research in this sector. However, silicon-based technologies now face problems arising from the high pressure of miniaturization. The research of new semiconducting materials is therefore gaining increasing attention. Especially with the rapid development of methods enabling super clean, and precise preparation of semiconductor materials (MBE, MOCVD), semiconductor alloys are also beginning to come to the forefront of the scientific community's interests. One of the most widely researched compounds combine elements of group III and elements of group V. For this reason, they are referred to as III-V semiconductors. Individual III-V semiconductors differ in their specific properties and cover, therefore a wide range of applications. The most commercially used III-V semiconductors are currently GaN, InP, GaAs, InAs, InSb. With the constant pressure on down scaling of devices and technology in general, low-dimensional III-V nanostructures of unique shapes are gaining importance for specific applications.

Such structures may be, for example, nanowires, which have specific properties given by their size, shape, large surface to volume ratio, and more. Nanowires are quasi one-dimensional nanostructures. The nanowires length can reach micrometers while their typical diameters range in the order of tens of nanometers. III-V nanowires thus have an outstanding potential as building blocks for novelty technologies since they combine the properties of III-V semiconductors and unique properties of nanostructures. For the integration of nanowires into devices or for the development of new applications using nanowires, it is therefore necessary to master their fabrication and understand the effects of the fabrication process on their properties.

The diploma thesis gives a brief introduction to the theory of III-V semiconductors. The following text discusses the fabrication of semiconducting nanostructures in the form of nanowires. The main attention is focused on the mechanism of their formation and on two theories explaining their growth, namely, selective area epitaxy and vapour-liquid-solid mechanism. The next chapter summarizes the most important experimental techniques used for the fabrication of III-V nanostructures presented in the thesis. The largest part is dedicated to molecular beam epitaxy (MBE) as the crucial method for their fabrication. The text continues with a short introduction to scanning electron microscopy (SEM) and its

usage for electron beam lithography (EBL). Experiments presented in the thesis focus especially on indium arsenide as III-V semiconductor with extremely high charge carrier mobility, making it an outstanding candidate for the semiconductor industry. The experimental part of the thesis presents in detail the vacuum apparatus utilized for the nanowire growth. The chapter continues with the discussion about indium catalyst preparation for self-catalyzed InAs nanowires via VLS mechanism. The biggest space is dedicated to experiments presenting the growth of indium arsenide via SAE mechanism. The first part presents nanowires grown on a silicon substrate with thermally decomposed native silicon dioxide. The second part presents the combination of electron beam lithography and wet chemical etching for the preparation of patterned SiO_2 used for the growth of precisely positionally controlled InAs nanowires.

2 THEORETICAL BASIS

2.1 Semiconductors

A semiconductor is usually defined as a material with electrical resistivity lying in the range of 10^{-2} – $10^{9}\,\Omega$·cm [1]. Its resistivity ranges between that of a conductor and an insulator and at the same time, unlike in metals, decreases with increasing temperature. Alternatively, semiconductor can be defined as a material whose energy gap for electronic excitations lies between zero and about 4 eV [1]. For better understanding of the difference between metals, semiconductors and insulators, and understanding the concept of band gap, it is necessary to look at materials from the perspective of quantum mechanics and investigate energy states of electrons.

Electrons are quantum objects with the wave particle duality character and are uniquely characterized by four quantum numbers n,l,m,m_s. According to laws of quantum mechanics, electrons can exist in atoms exclusively on specific discrete energy levels. When atoms are brought together to form solid matter, due to the Pauli exclusion principle, the existence of multiple electrons with the same ensemble of quantum numbers on the same certain energy level is forbidden. The levels start to split into quasi continuous energy bands. The formation of energy bands is schematically shown in 2.1.

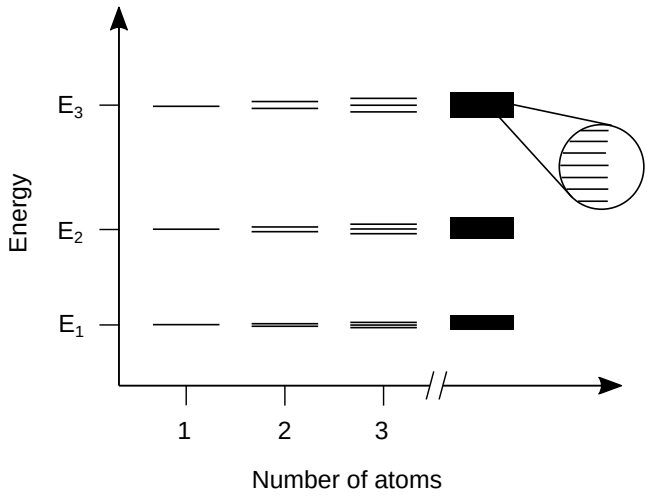


Figure 2.1: Schematic drawing of energy bands formation. As soon as individual atoms begin to form solid matter, electron energy levels start to split according to the laws of quantum physics and form quasi continuous energy bands.

The highest occupied energy level at temperature $T = 0\,\mathrm{K}$ is called Fermi energy. Thus applies that at $T = 0\,\mathrm{K}$ all energy states below Fermi energy level are occupied and all above are empty. The first energy band below the Fermi level is named as valence band. The first energy band above the Fermi level is then named conduction band.

Solid materials can be categorized into specific groups in accordance with the mutual position of the valence and conduction band. In metals, the valence and the conduction band overlap allowing electrons to contribute to conduction of electric current. In insulators, there is a significant gap of forbidden energies between the bands. This makes it almost impossible for electrons from valence band to get to conduction band since the energy band gap by far exceeds the thermal energy of electrons at room temperature.

The energy difference between valence and conduction band in semiconductors is smaller than in metals and electrons can be thus transferred, with a certain probability, into the conduction band and participate in conduction of current. Mutual position of valence and conduction band for metals, semiconductors and insulators is schematically shown in figure 2.2.

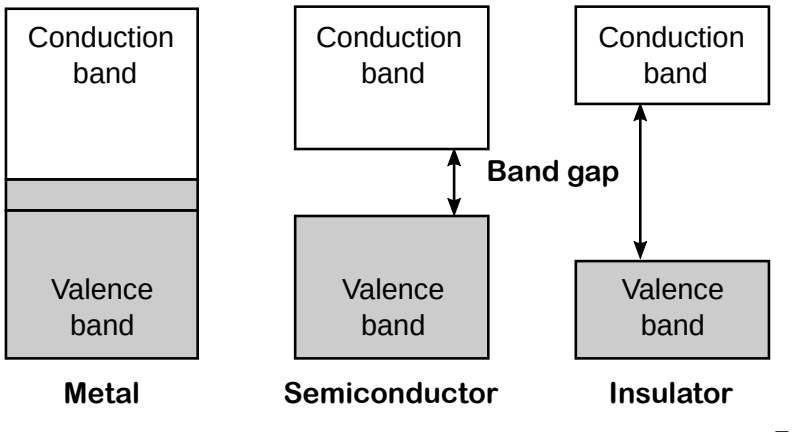


Figure 2.2: Schematic drawing of energy bands for the case of metal, semiconductor and insulator. Adapted from [2] and edited.

It is necessary to note at this point that the theory of semiconductors and band structure in solid state is actually far more complex and complicated physical phenomena working with concepts which are beyond the scope of this thesis. The theory as presented here is only a great simplification of the issue used to understand the basic properties of semiconductors. Further information about the topic may be found for example in [3].

The most industrially important semiconductor is undoubtedly silicon. It is an example of the so-called elemental semiconductor consisting of only one type of atoms. Germanium can be mentioned as an example of another elemental semiconductor. However, especially with the rapid development of methods enabling super clean and precise preparation of semiconductor materials, semiconductor compounds have come to the forefront of scientific community's interests. Binary, ternary or quaternary semiconductors combine two, three or four elements to form

semiconducting compound with new properties. Elemental semiconductors and semiconducting compounds differ in crystal phase, lattice constant, band gap characteristics and more. Therefore, they also cover a wide range of applications in light emitting diodes [4], transistor components [5, 6], optoelectronics [7, 8], gas sensors [9, 10] and in others. The figure 2.3 shows lattice parameter and band gap for some of the industrially important and most researched semiconductors.

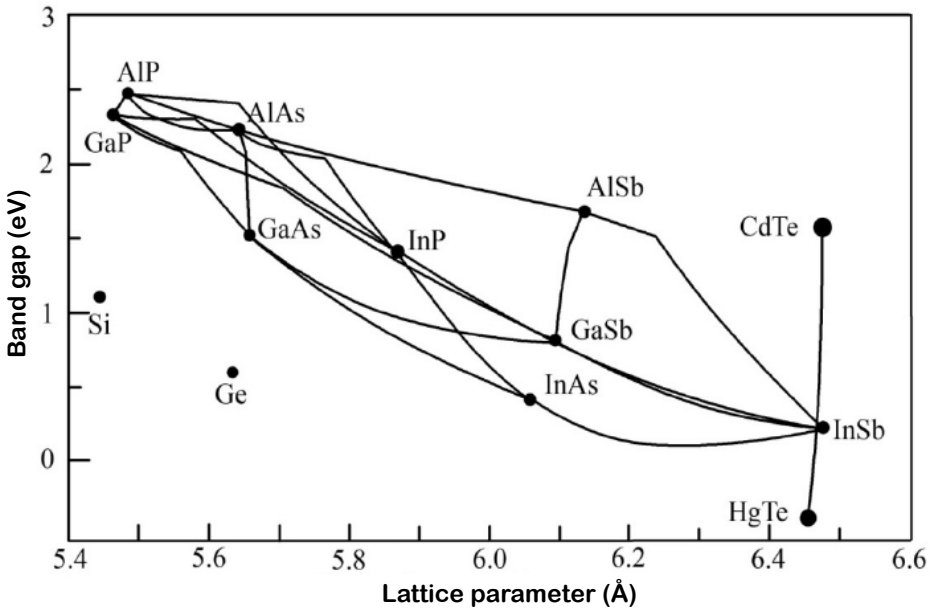


Figure 2.3: Lattice constant and band gap for most common semiconductors. Adapted from [11] and edited.

This master's thesis deals with binary semiconductors combining trivalent elements of group III and pentavalent elements of group V from the chemical table of elements. For this reason they are referred to as III-V semiconductors. Among the most common III-V semiconductors are GaN, InAs, GaAs, InP, InSb. The group of surfaces and thin films at the Institute of Physical Engineering has a dedicated vacuum chamber for the preparation of III-V semiconductors, mainly III-arsenides compounds. This thesis is especially focused on indium arsenide (InAs). The motivation for studying InAs from all III-arsenides lies in its high charge carriers mobility among not only III-arsenides but III-V compounds in general. High mobility makes InAs an excellent candidate for applications in low-power high speed electronics. The charge carrier mobility for some semiconductors is presented in figure 2.4.

As the name suggests, InAs is a compound of indium and arsenic. Indium (In) is an element of the group III of the periodic table of elements with atomic number 49. Arsenic (As) is an element of the group V of the periodic table of elements with atomic number 33. Indium arsenide has the appearance of gray crystals. It is a direct band gap III-V semiconductor with relatively small band gap of approximately 0.36 eV at 300 K. By its properties, it is similar to gallium arsenide (GaAs), another member of III-V semiconductors. The alloy system consisting of In, Ga and As in form of $In_xGa_{1-x}As$ is frequentelly used in band gap engineering since by the In and Ga components ratio

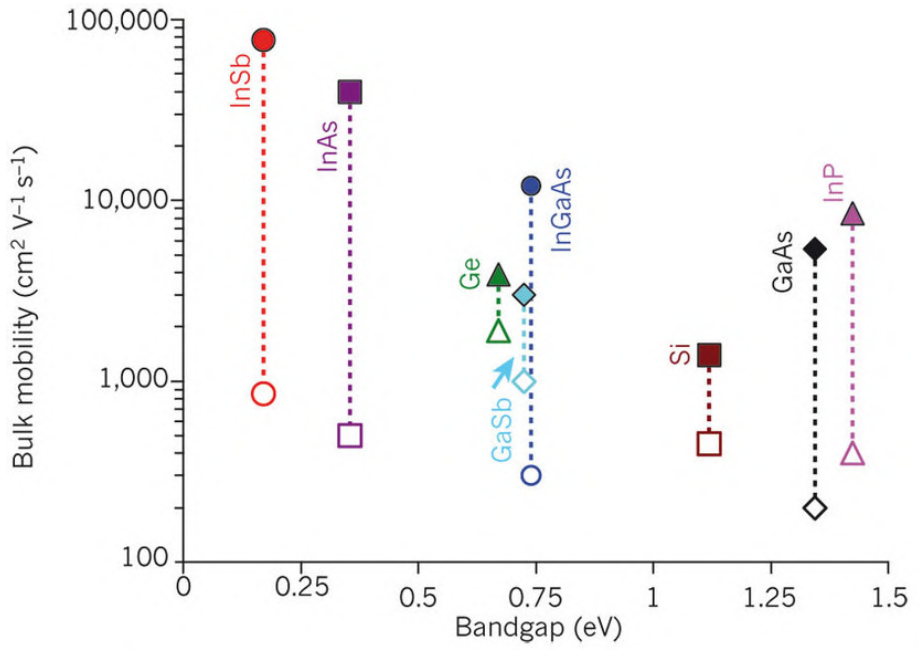


Figure 2.4: Bulk mobility of Si, Ge, and III-V materials with their respective energy band gap. The empty symbols are used for hole mobility, the solid symbols are used for electron mobility. Adapted from [12].

it is possible to precisely tune the exact energy value of band gap. Indium arsenide main application is as a substrate for a growth of mid-infrared LEDs and detectors and as magnetic field sensor [13]. Intrinsic InAs shows n type conductivity with a carrier concentration in the order $10^{16}\,\mathrm{cm}^{-3}$. Sulfur is used for n type doping. Zinc is used for obtaining p type conductivity. Carrier concentrations of up to about $10^{18}\,\mathrm{cm}^{-3}$ can be obtained for both n and p type doping [13].

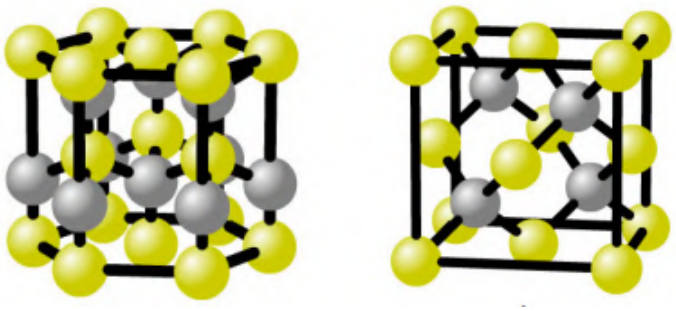


Figure 2.5: Hexagonal wurtzite (left) and cubic sphalerite (right) crystal modification of indium arsenide. Based on [14].

Bulk InAs crystallizes in cubic sphalerite (SF) configuration however hexagonal wurtzite (WZ) modification is often observed in nanoscale, for example in nanowires. InAs nanowires can be formed purely in either wurtzite or sphalerite crystal modification [16], but the occurrence of both phases is far more common. The lattice constant in WZ has the value of 4,26 Å and the lattice constant in SF is 6,06 Å [17]. The wurtzite structure is characterized by the repetition of two planes Aa and Bb. The sphalerite crystal modification can be described by alternating of three planes

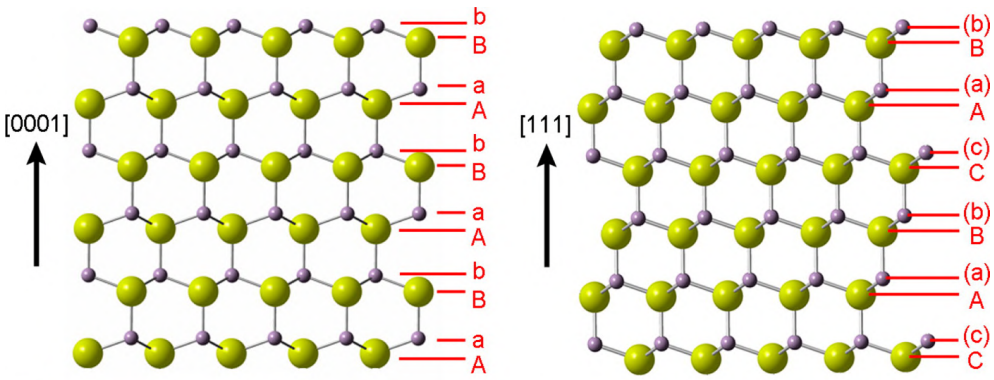


Figure 2.6: Hexagonal wurtzite (left) and cubic sphalerite (right) crystal modification of indium arsenide. The hexagonal structure is characterized by alternating of two planes Aa, Bb. The cubic structure is typical by altering three planes Aa, Bb and Cc. Yellow color represents indium atoms, grey color arsenic atoms. The arrows show the growth direction with corresponding Miller index. Adapted and edited from [15].

Aa, Bb, Cc. In both cases, the upper letters indicate indium atoms position and lower letters indicate position of belonging arsenic atoms. The anomaly in the regular alternation of layers is referred to as stacking fault and is one of the most common crystal lattice defects in InAs nanowires [18, 19].

Due to the pressure on constant downsizing and better performance of the electronic devices, more and more attention is paid to nanostructures of specific shapes. Combination of III-V semiconductors and nanoobjects of specific shapes therefore offers wide range of potential applications based on novelty principles.

The practical part of this work is aimed at III-V semiconductors in the form of nanowires, the next chapter is therefore devoted to these one-dimensional structures.

2.2 Nanowires

Nanowires are quasi one-dimensional nanostructures. This means their radial dimension is far smaller than their length. The typical diameter of nanowires is in the order of tens to hundreds of nanometers, while their length can reach tens of micrometers. Such nanostructures are therefore potentionaly interesting due to their specific properties like large surface to volume ratio [20, 21], lattice strain relaxation [22, 23], quantum behaviour [24] and more. Other applications are then based on the combination of III-V semiconductors and 1D structures. Specific properties based on this combination have already been studied for many materials. Examples are nanowires from GaN [25, 26], GaAs [27, 28], InP [29, 30], InSb [31, 32] and more. This chapter first introduces the surface processes necessary for understanding of nanowires formation and then briefly summarizes two basic physical descriptions of nanowires growth. One is vapour-liquid-solid (VLS) mechanism and the other is selective area epitaxy (SAE) mechanism.

2.2.1 Surface processes related to nanowires growth

The behaviour of atoms on the substrate surface is a crucial aspect determining the character of the resulting nanostructures. This section briefly discusses the processes on the substrate surface during the deposition by, for example, molecular beam epitaxy. Multiple physical phenomena can occur after the deposited atoms reach the substrate. There is a schematic representation of the most important ones in figure 2.7.

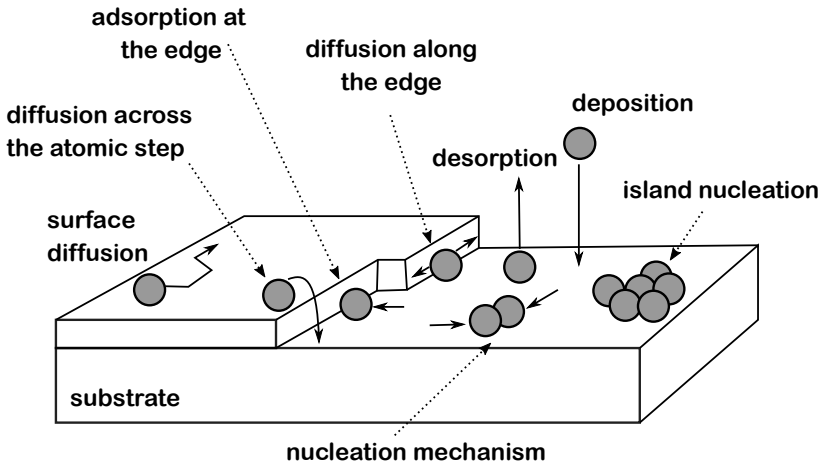


Figure 2.7: Behaviour of deposited atoms on the substrate surface. Adapted from [33] and edited.

The deposited particle diffuses over the surface of the heated substrate until it desorbs or it is integrated into existing or newly formed layers. Physically adsorbed atom can diffuse on the substrate because it is only weakly bonded. Chemically

adsorbed atoms create a chemical bond with the surface and their probability of desorption is then lower. Whether the atoms bind to an atomic step or start to cluster into individual islands is an interplay of many factors: substrate temperature, the number of atoms diffusing across the surface, diffusion coefficient, sticking coefficient and many more. The combination of all above-mentioned processes leads to the resulting mechanism by which the new material crystallizes on the substrate. There are three different ways how a new layer is formed as described in [34].

- Frank–Van der Merwe mode - also known as layer-by-layer growth
  Adatoms from the vapour supply are bonded preferentially to atomic steps resulting in smooth, continuous layers.

- Stranski–Krastanov mode - also known as combined growth
  Both 2D layer and 3D island growth occur during this intermediary process. Transition from layer-by-layer to island-based growth is highly dependent on the chemical and physical properties, such as surface energy and lattice parameters.

- Volmer–Weber mode - also known as island growth
  The interactions between atoms of the vapour supply are stronger than their interactions with the surface. This leads to the formation of three-dimensional islands.

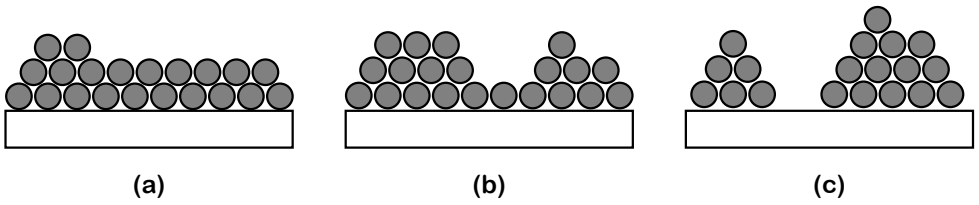


Figure 2.8: Schematic representation of three growth mechanisms. Frank-Van der Merwe (a), Stranski-Krastanov (b), Volmer-Weber (c) growth mechanism.

The above described surface processes are crucial for understanding of nanostructure formation on crystalline substrates. In the following text, the phenomena discussed here serve to explain the basic methods of nanowire growth. Specifically, the mechanism of selective area epitaxy which explains the formation of nanowires on substrates without the use of a catalyst is presented. It is followed by a section about vapour-liquid-solid mechanism which explains the growth of nanowires from catalysts.

2.2.2 Selective area epitaxy mechanism

The selective area epitaxy (SAE) mechanism does not utilize any catalyst and is only possible on substrates with an oxide surface layer. In the case of silicon, this role is often played by the native SiO_2. The nanowire growth is possible due to the presence of imperfections in the oxide layer. These are fabricated by etching of the substrate or by its heating above the oxide decomposition temperature. Both approaches lead to partial decomposition of the oxide layer and formation of pinholes. The resulting defects on the surface act as nucleation centers for atoms deposited on the sample. Deposited atoms diffuse over the substrate surface until they reach the imperfections. Nanowires are then formed in these places. The fact that growth continues one-dimensionally, in contrast to lateral overgrowth, is attributed to the formation of slowly growing side facets with a low surface energy [35]. The fast growth of the nanowire top facet and the slow growth of the side facet with lower surface energy therefore causes significantly faster growth in one direction. The nanowire tend to nucleate preferentially at the pinhole edge. The radial growth of the nanowire is then limited by the size of the oxide layer opening. Atoms are added to the forming nanowire by diffusion along its sidewalls. The length is determined mainly by the time of deposition. A schematic illustration of the SAE mechanism is shown in 2.9.

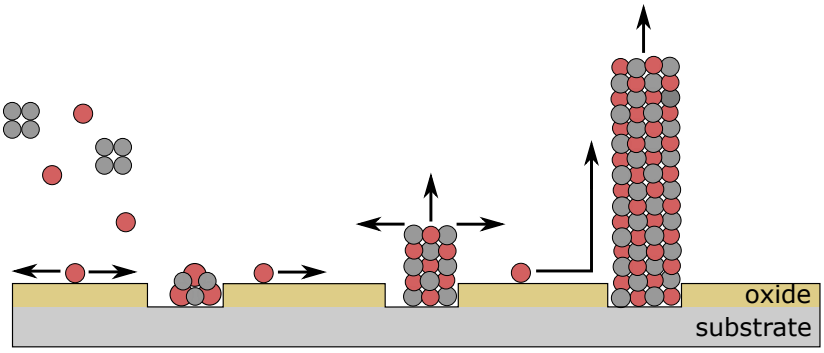


Figure 2.9: Selective area epitaxy mechanism of nanowire growth. Redrawn and edited from [36].

The etching of the oxide layer can be performed through a lithographic mask. It results in a fabrication of nanowires with precisely defined diameters and positional control. This approach is presented, for example, in [37, 38]. By changing the dimension of mask openings (diameter, depth), it is possible to influence the nanowire diameter or, for example, the number of nanowires growing within one mask opening [39]. InAs nanowires grown on patterned SiO_2 mask are shown in figure 2.10.

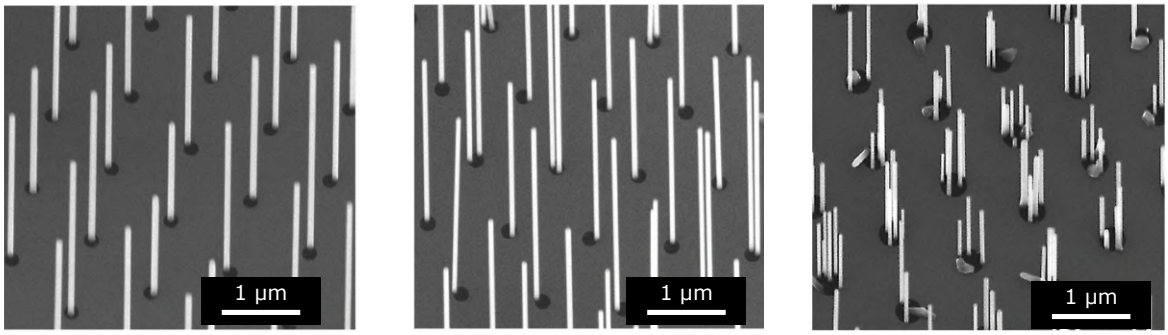


Figure 2.10: Arrays of InAs nanowires. Mask opening were fabricated by the combination of electron beam lithography and wet chemical etching. Mask opening diameter is 165 nm (left), 185 nm (middle) and 300 nm (right). Adapted from [39].

Depending on the quality of the oxide layer, other pinholes or steps may be formed on the substrate surface. Spots on such rough surface can provide extra nucleation sites besides the patterned mask openings resulting in parasitic growth in other than desired areas. Nanowires grown on thermally decomposed layers are often accompanied by this phenomenon as thermal decomposition cannot usually be precisely controlled. For the same reason, nanowires produced by this approach exhibit often high dispersion of diameters and length. An example of InAs nanowires fabricated on thermally decomposed SiO_2 is shown in figure 2.11.

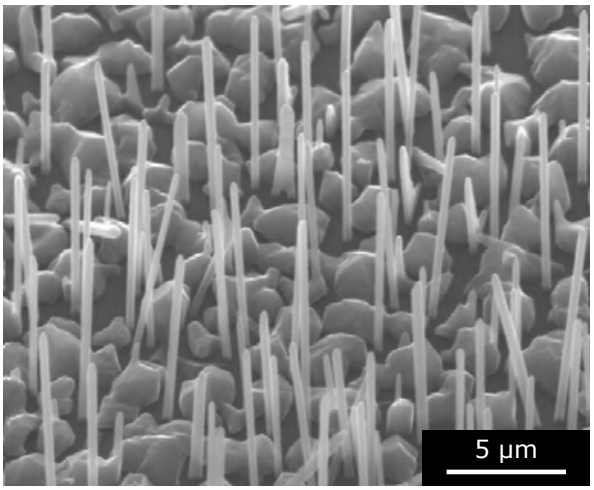


Figure 2.11: InAs nanowires grown on silicon substrate with thermally decomposed SiO_2 layer. Adapted from [40].

Focused ion beam (FIB) can be also used for the preparation of well-defined preferential nucleation spots, in addition to the above-mentioned methods, as presented, for example in [41, 42]. Another technique used is nanoimprint lithography [43].

2.2.3 Vapour-liquid-solid mechanism

This physical model was first presented in 1964 [44] where it was used for explanation of silicon nanowires growth using gold catalytic particles. Since then, it has been widely accepted and used for explaining the formation of nanowires from catalytic droplets. The catalysts can be metal nanoparticles. Gold and silver are mostly used for III-V semiconductors. The resulting nanowires are referred to as foreign metal-seeded. One of the nanowire constituent elements can also be used for catalyzing growth. Such nanowires are called self-seeded. A droplet of element III is usually used for catalysis in case of III-V nanowires.

Catalytic particles are prepared on substrate in several ways.

- colloidal nanoparticles
  Colloidal nanoparticles are transfered onto the substrate surface from colloidal solution. The advantage is an easy preparation and unified particle size. On the other hand, the distribution of the particles on the substrate is random and it is thus not possible to influence the exact position of the particles. Therefore, the position of the formed nanowires cannot be controlled either. However this method is not suitable for preparation of catalyst for self-seeded III-V nanowire growth.

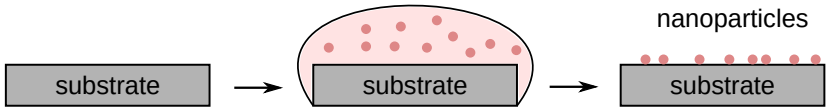


Figure 2.12: Preparation of substrate with colloidal nanoparticles.

- ripening of continuous layer
  A thin layer of catalyst material is evaporated on the substrate. The layer is heated which causes decomposition into individual islands. The size and areal density of the particles can be partially controlled by the thickness of the deposited layer and by the temperature used for decomposition. However the method will always result in randomly placed particles of different size. The method is applicable for preparation of foreign metal-seeded as well as self-seeded nanowires.

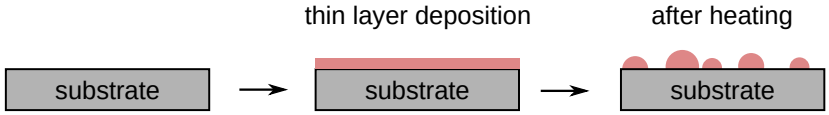


Figure 2.13: Preparation of catalytic nanoparticles by heating.

- litographically fabricated nanoparticles
  A lithographic pattern is first formed on the substrate. Afterwards, the catalyst material is deposited. There are nanoparticles of well defined dimensions and position on the substrate after lift-off process. This approach is very time consuming but results into precise control of position and size of catalyst. It can be used for fabrication of catalysts for metal-seeded and also self-seeded nanowires.

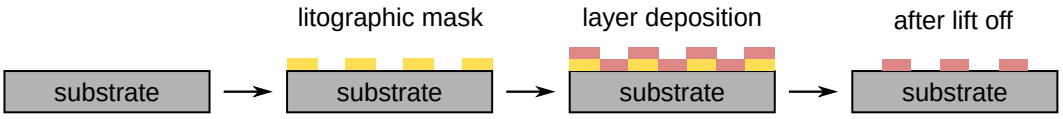


Figure 2.14: Preparation of catalytic nanoparticles using electron beam litography.

After the catalytic particles are prepared on the surface, the substrate is heated so they come into a liquid phase. Atoms or molecules of the resulting nanowire are deposited on the substrate. The catalyst serves as a collector in which the atoms dissolve. The droplet reaches a state of supersaturation when it is no longer able to accept new atoms of the dissolved material. The solid phase crystallizes at the droplet-substrate interface. The more in-detail description of the process is discussed in section 2.2.4.

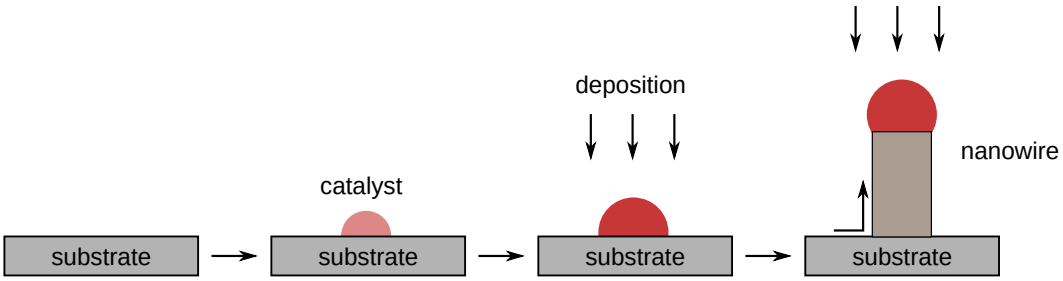


Figure 2.15: Vapour-liquid-solid mechanism of nanowire growth. A catalyst is formed on the substrate surface. The sample is heated and beam of deposited atoms is focused on the substrate. An alloy of catalyst and deposited material is formed. Deposited material precipitates under the liquid droplet and forms nanowire.

As it is evident from the description of the VLS mechanism, a typical feature of nanowires grown via this mechanism is a droplet of the catalyst, or more precisely an alloy of the catalyst and nanowire material, at the very top of each nanowire. This fact is visible in figure 2.16. However, the droplet may fall during growth and the resulting nanowires may lack this typical element eventhough they have grown via VLS. Various elements have already been used for catalysys of InAs. Nickel (Ni) [45], silver (Ag) [46] or palladium (Pd) [47] can be mentioned as examples. The use of gold-catalyzed and self-catalyzed nanowires nonetheless still remains the most widely preferred.

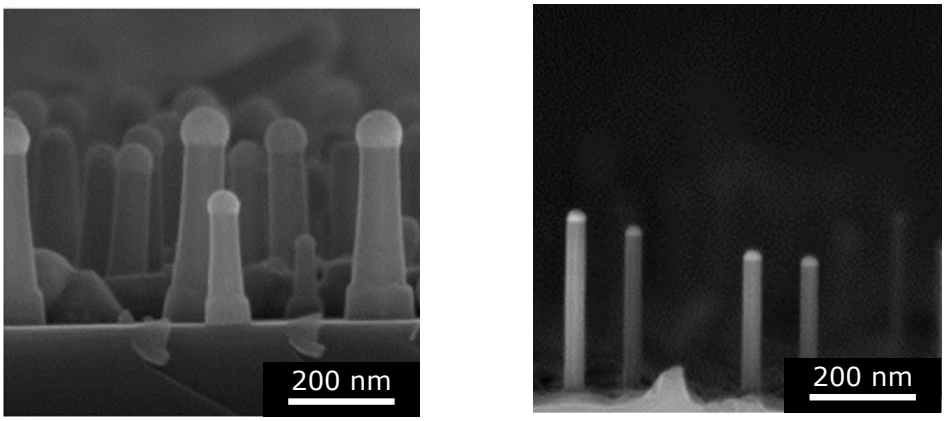


Figure 2.16: Indium arsenide nanowires catalyzed by pure indium droplet (left) and gold nanoparticle (right). Adapted from [48].

2.2.4 Nucleation theory

The thermodynamic driving force for crystal growth is supersaturation, which is defined by differences in chemical potential. After a liquid catalytic nucleus is formed on the solid substrate and the substrate is exposed to atomic vapour, there are three different segments in the system from the perspective of chemical potential. The solid crystal has a chemical potential of μ_{k}, the liquid droplet collector has a chemical potential of μ_{c} and the vapour supply is characterized by chemical potential μ_{s}. The point of contact of all three phases is called three-phase boundary (TPB). This physical system is schematically shown in figure 2.17. Supersaturations of individual interfaces are then defined by the change of chemical potentials of individual phases. The supersaturation between supply and collector is described as

$$\Delta\mu_{\mathrm{sc}} = \mu_{\mathrm{s}} - \mu_{\mathrm{c}}. \tag{2.1}$$

Whether the supersaturation is positive or negative describes the most probable behaviour of atoms on the particular interface. The atoms tend to move from places with higher chemical potential to places with lower. If $\Delta\mu_{\mathrm{sc}} > 0$, particles from the vapour are incorporated into the liquid collector. If $\Delta\mu_{\mathrm{sc}} < 0$, atoms are desorbed from the liquid collector into the vapour supply. For $\Delta\mu_{\mathrm{sc}} = 0$, the vapour-liquid interface is in equilibrium.

The supersaturation between supply and crystal phase is described as

$$\Delta\mu_{\mathrm{sk}} = \mu_{\mathrm{s}} - \mu_{\mathrm{k}}. \tag{2.2}$$

Similar to the above, for $\Delta\mu_{\mathrm{sk}} > 0$ the most probable way for particles is to be relocated from supply into the solid crystal. For $\Delta\mu_{\mathrm{sk}} < 0$, atoms desorb from solid phase into the vapour.

Finally, the supersaturation between collector and crystal phase is given by

$$\Delta\mu_{\mathrm{ck}} = \mu_{\mathrm{c}} - \mu_{\mathrm{k}}. \tag{2.3}$$

The different cases are analogous. Atoms move from collector to crystal if $\Delta\mu_{ck} > 0$. The case of $\Delta\mu_{ck} < 0$ describes the opposite process and for $\Delta\mu_{ck} = 0$, no atoms pass between the phases.

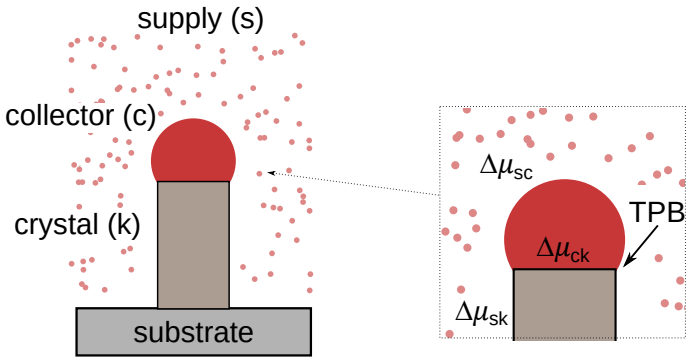


Figure 2.17: Supersaturation on different interfaces and three phase boundary position.

In the simplest approximation for VLS mechanism, the condition

$$\mu_s > \mu_c > \mu_k \tag{2.4}$$

must be fulfilled for the atoms to be reassigned from the gas supply through the liquid collector into the solid crystal phase. However, this condition is insufficient for the explanation of VLS nanowire growth. It does not answer the question why crystallization does not occur directly from the gas supply phase if the supersaturation $\Delta\mu_{sk}$ is patently higher than $\Delta\mu_{ck}$. For a full understanding of VLS growth mechanism, the change of Gibbs energy on the phase interfaces has to be taken into consideration. An approach involving this fact described herein is presented in [49]. The change of Gibbs energy on the gas-solid interface follows:

$$\Delta G_{sk} = -n\Delta\mu_{sk} + Ph\sigma_{sk}. \tag{2.5}$$

In a similar way, the change of Gibbs energy on the liquid-solid interface is given by:

$$\Delta G_{ck} = -n\Delta\mu_{ck} + Ph\sigma_{ck}, \tag{2.6}$$

where n is the number of particles transferred between phases, h is height of the nucleus, P is its perimeter length and σ_{sk} and σ_{ck} are the surface energies of the particular interface.

Last but not least, it is necessary to look at the change of Gibbs energy on the three-phase boundary. This follows:

$$\Delta G_{TPB} = -n\Delta\mu_{sk} + P_{sk}h\sigma_{sk} + P_{ck}h\sigma_{ck}, \tag{2.7}$$

where P_{sk} is the perimeter length of supply-crystal interface, P_{ck} is the perimeter length of collector-crystal interface. Only the highest supersaturation $\Delta\mu_{sk}$ is considered, according to condition 2.4, for simplification.

The surface energies of different interfaces are interrelated according to Young equation [50]

$$\sigma_{\mathrm{sk}} = \sigma_{\mathrm{ck}} + \sigma_{\mathrm{sc}} \cos\theta. \tag{2.8}$$

The parameter θ is called the wetting angle (sometimes also contact angle) and defines the geometry of the collector as it is schematically drawn in 2.18. From the Young equation 2.8 and figure 2.18 it is evident that for the wetting angle $\theta < 90°$ the surface energy of supply-crystal interface is higher than the surface energy of collector-crystal interface.

$$\sigma_{\mathrm{sk}} > \sigma_{\mathrm{ck}} \tag{2.9}$$

and vice versa for the wetting angle $\theta > 90°$

$$\sigma_{\mathrm{sk}} < \sigma_{\mathrm{ck}}. \tag{2.10}$$

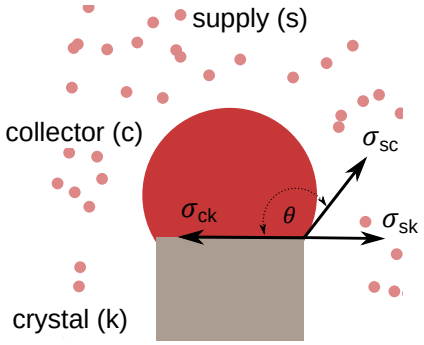


Figure 2.18: Scheme of the wetting angle on TPB and layout of interaction from all interfaces.

By comparing equations 2.6, 2.5 and 2.7, it is possible to predict at which interface the nucleation starts with the highest probability. Nucleation most likely occurs at the place the change in Gibbs energy ΔG is minimal. In other words, ΔG is there the most negative. At the TPB, the change in Gibbs energy for the formation of a nucleus could be very low because the supersaturation $\Delta\mu_{\mathrm{sk}}$ is high. The nucleus shape and position can also adjust, so the edge energy terms have flexibility and can be thus minimized [49]. This high flexibility enables the minimization of Gibbs energy and makes TPB a preferential point of nucleation. The precipitation of the solid phase from the liquid phase starts at TPB and continues on liquid-solid interface until a new layer is formed. Continuous repetition causes the nanowire growth. The process of crystallization during VLS growth is shown in figure 2.19.

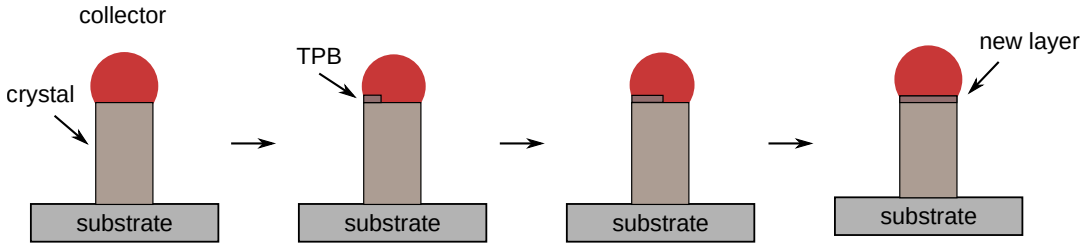


Figure 2.19: Forming of new layer according to vapour-liquid-solid mechanism. Crystallization occurs preferentially on tree phase boundary (TPB). The layer continues to grow on collector-crystal interface. Repetition of the process yields in nanowire growth.

3 USED METHODS

This chapter lists the experimental methods used in the work. The main space is dedicated to molecular beam epitaxy (MBE) as the most experimentally used and crucial method. The principle of scanning electron microscope (SEM) is also outlined as well as its usage for electron beam lithography (EBL).

3.1 Molecular beam epitaxy

Molecular beam epitaxy method was developed and highly improved during the late 1960s in Bell Laboratories [51]. Since then, it has become an indispensable fundamental technique used for the preparation of metals, oxides, and semiconductor compounds of ultra high quality. Unlike processes using precursors, for example, metal organic vapor phase epitaxy (MOVPE), MBE is considered one of the cleanest methods as the growth takes place in an ultra high vacuum (UHV). UHV environment is characterized by a pressure lower than 10^{-7} Pa [52]. Schematic representation of the molecular beam epitaxy apparatus is shown in figure 3.1.

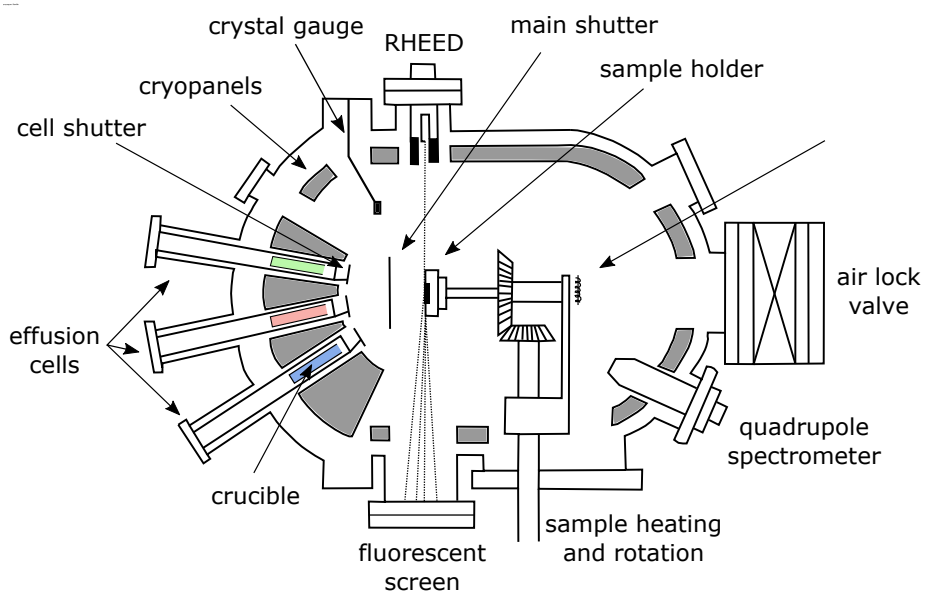


Figure 3.1: Picture of standard MBE chamber setup. Adapted from [53] and edited.

Low pressure provides a clean surrounding for epitaxial growth and minimizes the possibility of contamination of the fabricated structures with unwanted elements from the residual gas atmosphere. The MBE vacuum chamber usually contains several

evaporation cells. The schematic figure of an evaporation cell is shown in 3.2. The materials are stored in ultra pure solid form in crucibles placed near the opening of the cell. Crucibles are heated up until the point the given element reaches evaporation or sublimation. The evaporated atoms are focused by the collimator and enter the chamber in the form of a narrow beam. The beam intensity is controlled by the effusion cell temperature. Evaporation cells can be heated in multiple places. Secondary heating decomposes the bigger molecules coming out of the cell into individual atoms or smaller fractions. The heating is in most cases computer controlled. The temperature can be thus controlled with an accuracy of up to one degree Celsius using PID regulation. The cooling of the cell is usually ensured by flowing water.

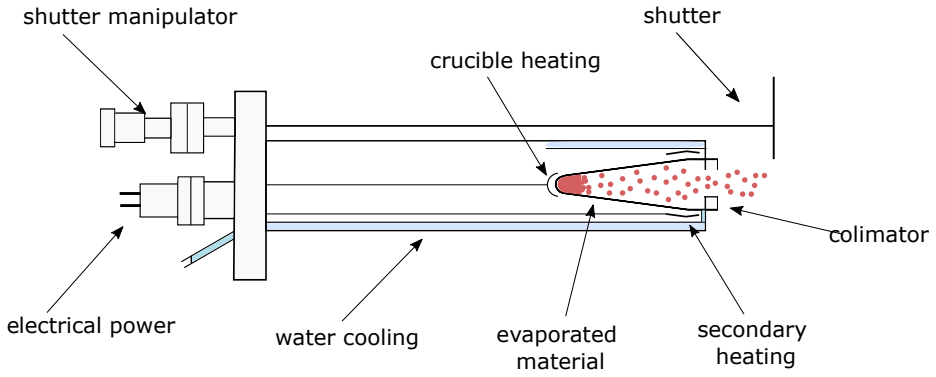


Figure 3.2: Schematic picture of standard effusion cell.

The mean free path between collisions of atoms and molecules in the beam is larger to the typical dimensions of the chamber. Under this condition, atoms and molecules interact only after they reach the heated substrate [54]. To ensure uniform growth, the holder with substrate can continuously rotate during the deposition. The special merits of MBE technique are that thin films can be grown with precise control over thickness, alloy composition, and doping level [55]. Using mechanical shutters controlled by computer, the composition of compounds can be changed abruptly and sharp interfaces or doping with extreme precision can be performed.

The MBE chambers often include methods for monitoring the growth process on the substrate in real time. One of the most used is the reflection of high energy electron diffraction (RHEED). Electrons produced by the electron gun hit the surface under a small angle. The electrons diffract on the upper layers of the grown material and create a diffraction pattern on the phosphor screen. From the diffraction pattern, it is possible to conclude the crystalografic phase or growth mechanism characteristics.

In addition to the above mentioned, MBE chamber usually contains gauges monitoring the vacuum level and particle beam flux. The deposition rate may be also measured by a quartz crystal. The crystal changes its resonance frequency during deposition. The change in frequency is proportional to the number of deposited particles of a defined mass.

3.2 Scanning electron microscopy

A scanning electron microscope (SEM) is a scientific instrument enabling direct observation of nano and microstructures. SEM uses electrons as an imaging probe in contrast to photons in a classical optical microscope. Primary electron beam is produced by the electron source. The electron beam is usually accelerated to energies in the range of (0.5-30) keV [56] towards the sample. The system of electron optics is used for focusing the electrons into the spot with small diameter. The interaction of electrons with the sample results in various outcomes. The most used signals for imaging are secondary (SE) and backscattered electrons (BSE). Secondary electrons are electrons from the sample produced by inelastic scattering of primary electrons. Their energies usually do not exceed 100 eV. Backscattered electrons are the primary electrons reflected from the sample. Another particles leaving the sample as a product of interaction with the primary electron beam are Auger electrons (AE), X-ray photons, or photons of visible light. Particles are collected by detectors and converted by a computer into signal intensity. Different signals can carry different information about the sample. Secondary electrons are often used for obtaining data about topography. The BSE signal offers chemical contrast since the BSE yield increases with the atomic number of the specimen [57]. The visual output from the microscope is achieved by scanning the focused beam point after point across the sample. The signal intensity is assigned to individual pixels in the form of intensity and a greyscale picture is formed.

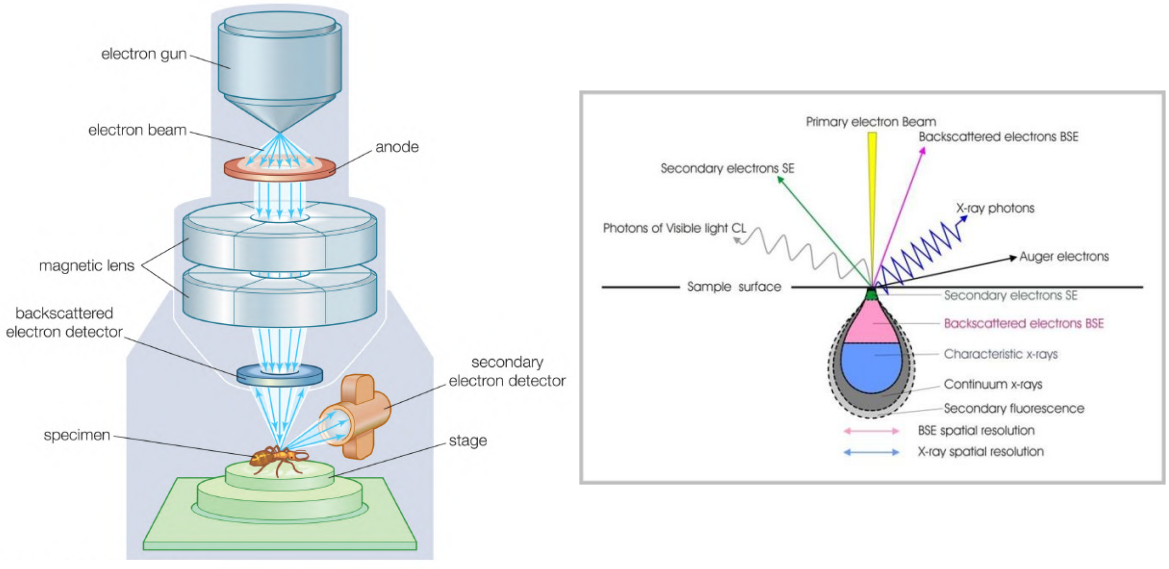


Figure 3.3: A simplified schema of scanning electron microscope. The primary electron beam is produced by electron source. It is accelerated and focused by electron optics. The interaction with the specimen leads into specific signals. Different particles leaving sample after interaction with depth of origin scheme. Adapted from [58] and [59].

3.3 Electron beam lithography

Electron beam lithography is a nanofabrication method using an electron beam for the fabrication of custom patterns on the substrate covered with an electron-sensitive chemical film called a resist. So called spin-coating method is used for covering the sample with resist. The sample is first heated for adsorption of water coming from air humidity. The resist is then pipetted on the clean substrate. Subsequently, the sample is spinned at high frequency causing the resist to be evenly distributed over its surface and forming a uniform layer. The resist covered sample is afterward baked out. Such a sample is ready for electron beam patterning. The electron beam causes a chemical change in the composition of the resist in places exposed to the accelerated electrons. The chemical change makes the exposed resist more soluble or, conversely, more resistant to a chemical substance called developer. In the case of positive resist, the chemical bonds in the resist are broken due to interaction with electrons and the irradiated areas are subsequently easily dissolvable in the chosen developer. In the case of negative resist, more resistant chemical bonds are created in the exposed areas making it less dissolvable in developer. Exposing the sample to the developer then leads to fabrication of specifically designed patterns of the remaining resist on the substrate. Mechanism of electron beam exposure for both positive and negative resist is schematically shown in figure 3.4. Polymethyl methacrylate (PMMA) is one of the most widely used electron beam lithography resist. Its advantages include high resolution and very low price. PMMA is produced in a wide range of modifications differing in polymer chain length and thus also specific properties for lithographic usage.

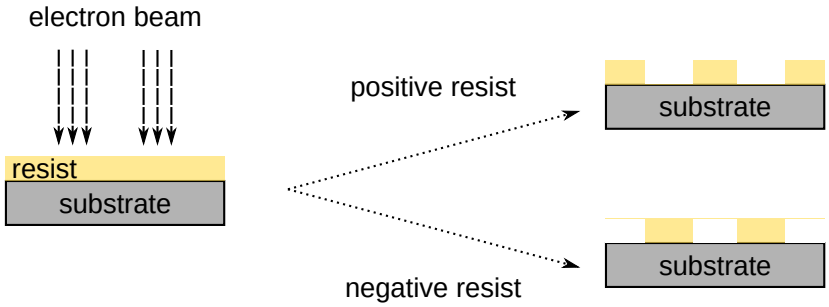


Figure 3.4: Scheme of electron lithography exposure using positive respective negative resist.

After predefined electron beam irradiation and selective removal of the resist by the developer, a material is added (i.e., by evaporator) to the uncovered place or removed (i.e., by etching) from the uncovered place. Two possible approaches of substrate modification using electron beam lithography are shown schematically in figure 3.5.

Compared to traditional projection optical lithography, electron lithography provides higher resolution and does not require the physical creation of masks, as the structure formed is directly rendered by the electron beam scanning system. Using this method, it is thus possible to produce patterns on a large-scale surface with extremely high details. The main disadvantages, however, are the low speed and the

need of organic chemicals used in the form of resist, which often reduce the cleanness of the sample. Electron beam lithography is currently mostly used for the fabrication of masks for optical lithography, low volume production of semiconductor devices, and research and development.

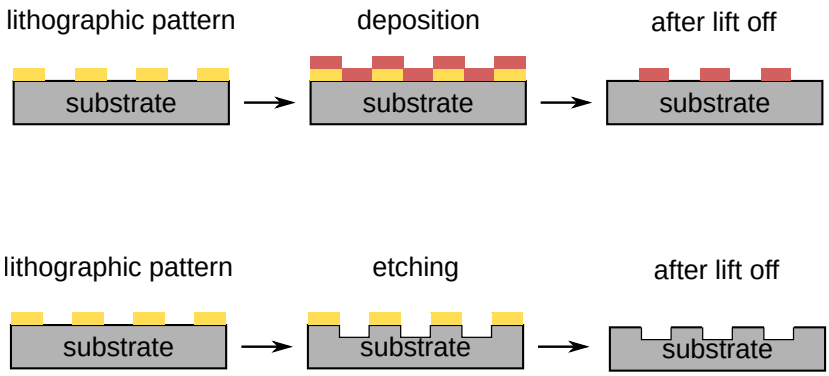


Figure 3.5: Two possible approaches of creating structures using electron beam lithography. Adding material by deposition. Removing the material by etching.

4 EXPERIMENTAL RESULTS

The experimental part of the diploma thesis was focused on the preparation of indium arsenide (InAs) nanostructures mainly in the form of nanowires. The chapter presenting the experimental results is divided into sections describing the experimental setup and used equipment, preparation of the catalyst for VLS growth and into a section describing SAE growth of InAs on both unpatterned and patterned substrates.

4.1 Experimental setup

Most of the experiments presented in this work were performed in the MBE vacuum chamber which is part of the UHV cluster of CEITEC Nano research infrastructure. As this work is focused on indium arsenide (InAs), two effusion cells were used during the work, namely, indium effusion cell and arsenic effusion cell. The indium effusion cell uses double heating for evaporation. Ultrapure indium is stored in a crucible. The crucible is heated at the bottom and at the same time separately at its opening. The opening of the cell is covered by a mechanical shutter. The opening and closing of the shutter are controlled by a computer as well as the heating temperatures of the effusion cell. The construction of the arsenic cell is slightly different from the indium one. Ultrapure arsenic is again stored in an inert crucible. The crucible is heated up by primary heating at the bottom and by secondary heating at the top of the cell. The main design difference lies in the use of a needle valve. The flow of arsenic is thus regulated by the mechanical insertion of the needle into the mouth of the cell. This process is also not computer automated due to low reliability. The sample is placed in a sample holder that enables heating controlled by the computer. The parameters defining the experiment are thus indium flux defined by the indium effusion cell temperature, arsenic flux defined by the arsenic effusion cell temperature, substrate temperature, deposition time, and chamber pressure. The experimental parameters are presented in the text in the following format:

- $T_1(\mathrm{In})/T_2(\mathrm{In})$ = indium effusion cell temperature (bottom/top of the cell)
- $T_1(\mathrm{As})/T_2(\mathrm{As})$ = arsenic effusion cell temperature (bottom/top of the cell)
- T_s = substrate temperature
- t = deposition time
- p = pressure

At this point, it should also be noted that some of the experiments were performed without the presence of an arsenic effusion cell in the MBE chamber. These are the experiments in the section 4.2. The time during which the cell was serviced by the manufacturer was used for these experiments. The conditions, especially regarding pressure, for the experiments performed with and without the arsenic effusion cell are significantly different. This is mainly due to the atypical behavior of evaporated arsenic in the operated UHV apparatus. Evaporated arsenic atoms are not focused in the form of a narrow beam similar to indium. The arsenic atoms tend to fill the entire chamber equally by its partial pressure. At the same time, mainly due to the low pumping speed of the dedicated vacuum system, it is not possible to reduce the arsenic partial pressure below a certain level. The base pressure inside the chamber without the presence of the arsenic effusion cell can reach the order of 10^{-10} mbar. After implementation and heating the arsenic cell, the vacuum pumping system is not able to reach a pressure below 10^{-8} mbar. The experiments, except those described in section 4.2, were therefore performed under non negligible arsenic partial pressure.

4.1.1 Calibration

For the repeatability and relevance of experiments, it is crucial to make a calibration of the experimental system. This ensures the values inserted into the computer software (temperature, atomic flux) correspond to the reality. Therefore, the temperature of the sample holder was measured using a pyrometer and the measured values were compared with the temperature values shown by the computer. The calibration result is presented in figure 4.1. The indium effusion cell calibration was also performed to determine the temperature dependence of the deposition rate of indium atoms as well as the indium partial pressure. This measurement was performed using a quartz crystal and beam flux monitor gauge as described in 3.1. The result is again presented in the figure 4.1.

The calibration of the sample holder temperature confirms that the real temperature differs from the temperature shown by computer and the temperature presented by the instrument software is thus not exactly accurate. This fact can be caused by the poor contact between the heater and the molybdenum sample holder. Heat transfer thus occurs not only by conduction but also by radiation which causes heat loss. Since this work serves as a set of technological procedures for the specific equipment, the temperatures of the holder entered into the software controlling the computer are presented in the text. However, it must be taken into consideration that the real values differ according to the calibration in figure 4.1.

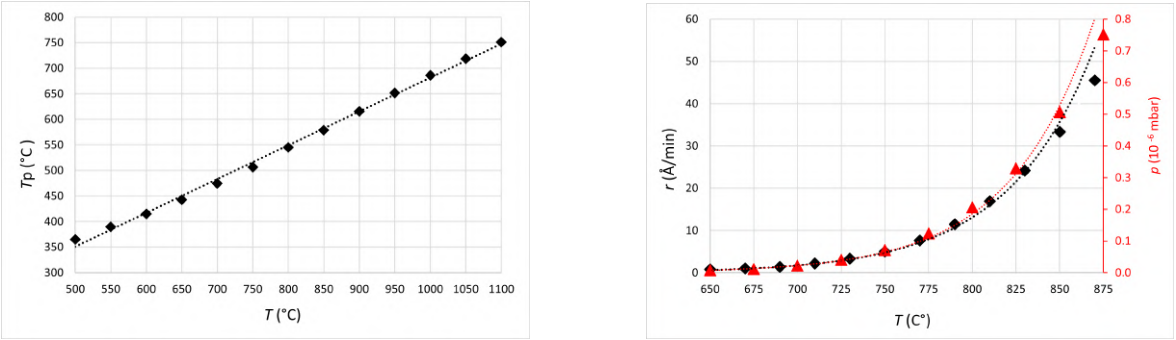


Figure 4.1: Calibration of sample holder temperature and indium flux. Left image represents dependence of the sample holder temperature measured by pyrometer (T_p) on the temperature value displayed by computer. The data were fit by a linear trendline. Right image shows dependence of indium flux (r) on the indium effusion cell temperature (bottom heating). Pressure data (p) correspond with the measurement by beam flux monitor gauge, deposition rate corresponds with the measurement by quartz crystal. Exponential trendline was added for both to guide the eye.

4.1.2 Sample preparation

Silicon crystallographic orientation (111) was used as a substrate for all experiments. Small pieces, approximately 5×5 millimeters, were cut from the wafer. The silicon substrate was then cleaned for 5 minutes in acetone using an ultrasonic bath followed by a 5 minute ultrasonic bath in isopropylalcohol (IPA). The silicon pieces were rinsed in distilled water and finally cleaned by gas nitrogen. The substrate cleaning process is shown schematically in the figure 4.2. The cleaned silicon substrate samples were then loaded into the MBE chamber.

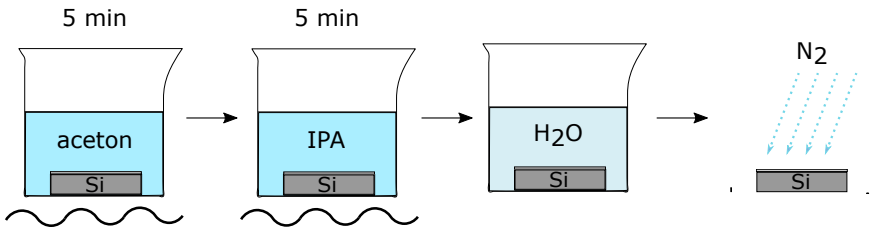


Figure 4.2: Schematic drawing of silicon substrate cleaning procedure. Cleaning consists of ultrasonic bath in aceton and IPA followed by cleaning in distilled water and by nitrogen gas stream.

4.2 Indium catalysts for VLS growth

The following section describes experiments aimed at the preparation of catalytic particles from pure indium for the preparation of self-seeded InAs nanowires by the VLS growth mechanism. The study of self-catalyzed III-V semiconductor nanowires is mainly important for their usage in the semiconductor industry. Metal free III-V nanostructures are nowadays highly preferred in this sector, as gold, widely used for the catalyzation of III-V nanowires, is incompatible with current silicon-based CMOS technology. This trend is followed in this thesis as well. However, the study of gold catalyzed InAs nanowires is also a subject of research in the Institute of Physical Engineering using the same MBE setup [60].

The experiments were performed in the absence of the arsenic effusion cell in the chamber. The influence of indium deposition parameters on the heated silicon substrate was investigated. The indium flux remains constant, so a constant number of indium atoms deposited on the surface was ensured. The main parameters guiding the formation of droplets are diffusion on the surface and adsorption.

The depositions were defined by the following parameters:

- $T_1(\mathrm{In})/T_2(\mathrm{In}) = 735/835\,^{\circ}\mathrm{C}$

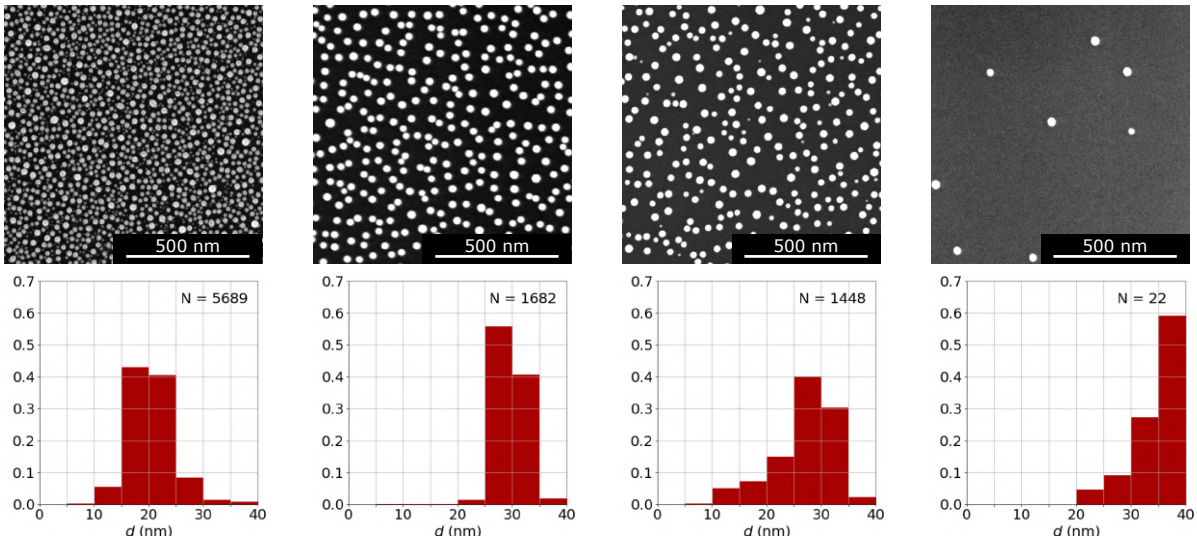
  (corresponding indium flux: $r(\mathrm{In}) = 2{,}6\,\text{Å/min}$)

- $T_\mathrm{s} = (500 - 600)^{\circ}\mathrm{C}$ (altered parameter)

- $t = 10\,\mathrm{min}$

- $p = (2{,}5 - 6{,}0) \cdot 10^{-9}\,\mathrm{mbar}$

The results of experiments with the stated parameters are shown in the figure 4.3. From the images, it can be estimated that the substrate temperature is a parameter that can affect the areal density and size of the indium catalytic nanoparticles. The experiments defined by the above stated parameters resulted in the formation of pure indium nanoparticles with diameters up to 40 nm. For the sample heated to a lower temperature ($T_s = 525\,^{\circ}\mathrm{C}$) during deposition, the areal density is clearly highest. The indium droplets occupy more than 40 % of the substrate surface. The particles also exhibit a high dispersion of their diameters. Deposition on substrates heated up to 550 °C and 575 °C resulted in coverage of the substrate with slightly bigger nanoparticles. The area coverage reached 17 % respective 14 % of surface area. Desorption already predominated in the sample heated to the highest temperature (600 °C). Particles were very rarely formed on the surface and covered less than 1 % of the sample surface. The statistical distribution over the particle diameters and areal density was done by ImageJ software plugin developed in [61] and a basic Python script and are presented in figure 4.3.



$T_s = 525\,°\mathrm{C}$ $T_s = 550\,°\mathrm{C}$ $T_s = 575\,°\mathrm{C}$ $T_s = 600\,°\mathrm{C}$

Figure 4.3: Indium catalytic nanoparticles after deposition on substrates with different temperatures. Flux of indium atoms was the same for all cases. The images were taken by FEI Verios 460L electron microscope. The bottom row presents a statistical percentage distribution of nanoparticles diameter. Images with view field of 2,5 × 2,5 µm were used for the statistical distribution evaluation. The total number of nanoparticles N is shown in the right corner of each graph.

The next experiment aimed to verify the possibility of preparing a pure catalyst in the presence of an arsenic effusion cell in the MBE chamber. The arsenic effusion cell was therefore installed in the chamber and tested. Already during the test heating of the cell it was evident that the vacuum system is not able to pump a sufficient amount of evaporated arsenic vapor. After the cell was switched off and cooled, the new base pressure stabilized at a low order of 10^{-7} mbar and after a few days of pumping in high 10^{-8} mbar. Two depositions were performed under the same parameters similar to those in figure 4.3. One with an open arsenic shutter and one with closed shutter for comparing the vacuum environment for both cases. The chamber pressure during deposition was low 10^{-6} mbar. The result is presented in figure 4.4.

It could be concluded from the images that during both cases there was a sufficient amount of arsenic vapor preventing formation of pure indium droplets. The result is most probably given by the InAs crystallization mechanism. Indium atoms diffuse over the heated substrate surface until they meet the arsenic atoms. Subsequently, indium arsenide crystallization occurs. Thus, with the increasing number of arsenic atoms near the substrate, the diffusion length of indium atoms along the surface decreases rapidly. If the partial pressure of arsenic particles exceeds a certain critical value, crystallization occurs almost immediately and pure indium clusters cannot exist in this environment for a sufficient time. Based on these arguments, it is more than probable that in this specific MBE chamber it is not technologically possible to prepare pure catalysts under standard conditions. Solution that could help is, for example, cooling the MBE chamber with liquid nitrogen to provide a higher vacuum. However, this is a very technologically demanding task, and in addition, rapidly prolongs any work and

therefore no attention has been paid to this idea.

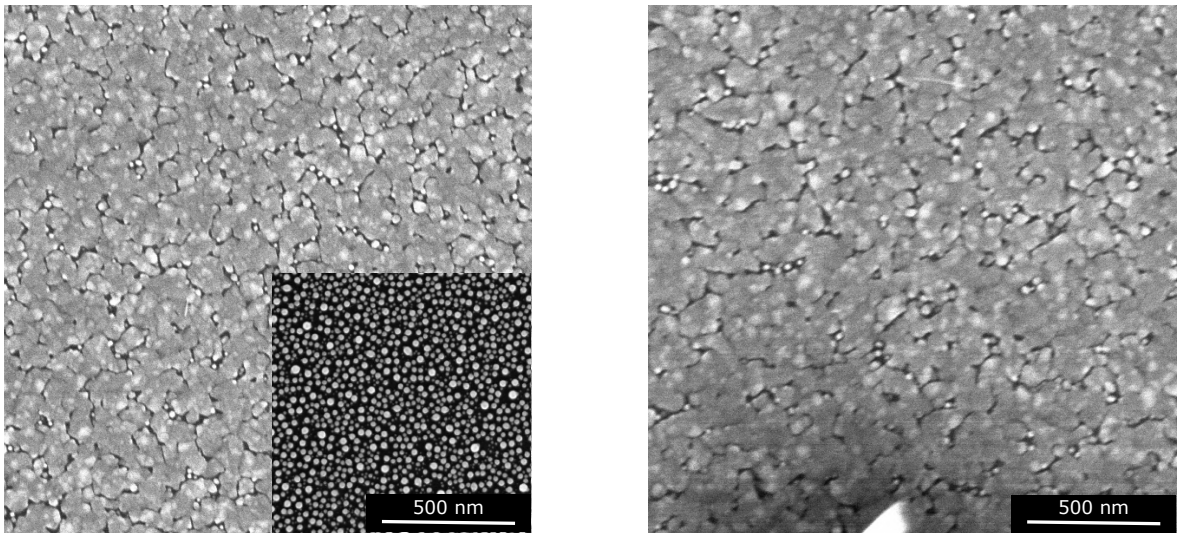


Figure 4.4: Two identical indium depositions performed with closed arsenic shutter (left) and opened arsenic shutter (right). InAs crystallized on both samples. The indium deposited without the presence of arsenic effusion cell is shown in the inset for comparison.

An X-ray photoelectron spectroscopy (XPS) analysis was performed on the samples presented in the figure 4.4 (left) to analytically confirm this hypothesis. Let's recall that the samples were prepared under similar conditions, the only difference being the absence of the arsenic cell in the chamber for the sample shown in the inset (pure indium deposition). The XPS measurement results are presented in the figure 4.5.

By comparing In 3d peaks of both measurements, it is possible to conclude that the sample prepared in an arsenic background pressure is predominantly covered by InAs. The indium signal is contrariwise predominant on the sample prepared under much higher vacuum. The peak is probably also slightly modified by InAs signal, because the presence of arsenic was also detected in this sample. However, due to the high noise in the corresponding arsenic signal and the ease of fitting, it was neglected. The XPS measurement was not executed immediately after withdrawing the samples from the MBE. The indium oxide signals therefore come from pure indium oxidation in the atmosphere. At the same time, according to the presence of strong arsenic signal, it can be stated that pure indium really cannot be prepared in a controlled manner in the presence of an arsenic effusion cell, which is nevertheless necessary for the possible indium catalyzed InAs nanowires fabrication. The arsenic signal was surprisingly detected even on the sample prepared without the presence of an arsenic effusion cell in the chamber. The source of arsenic atoms was apparently arsenic from previous experiments deposited on the walls of the chamber and the top of the remaining effusion cells. The arsenic residues then desorbed into the chamber simply by heating the indium effusion cell and the sample holder.

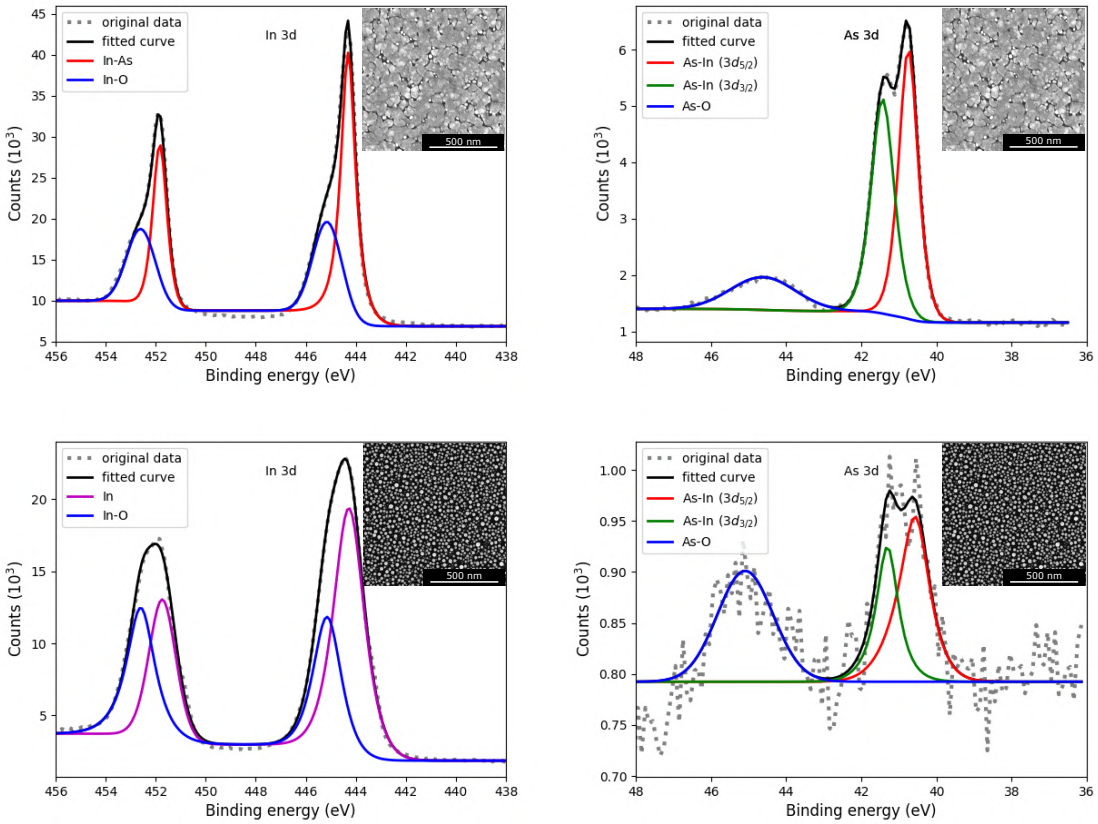


Figure 4.5: XPS spectra of indium deposition in arsenic vapour 10^{-6} mbar (upper row) and under significantly lower pressure 10^{-9} mbar (bottom row). Data published in [62, 63] were used as reference for XPS spectra interpretation.

4.3 SAE growth

Experiments presented in this section follow on the experiments of Ing. Tomáš Musálek on selective area epitaxy growth of InAs nanowires. The aim was also to repeat some previously performed key experiments to examine the reproducibility of the results over time. Silicon (111) with native silicon dioxide was used as a substrate. After the cleaning procedure, the sample was loaded into the MBE. The substrate was annealed at the temperature T_a for the time t_a, which was the investigated parameter. Annealing step ensures partial decomposition of the oxide layer and formation of microholes, which play a role of preferential nucleation places for deposited atoms. Annealing thus leads to a surface modification suitable for the nucleation of nanowires by the SAE mechanism as described in section 2.2.2. The arsenic effusion cell was always opened before the start of the experiment and after the pressure in the chamber had stabilized, a computer controlled recipe was started. After annealing the substrate, the sample holder temperature was reduced to T_s and the indium effusion cell shutter was opened. The deposition lasted for the time t_s. After this time, the indium cell shutter was closed automatically. The arsenic effusion cell shutter was closed manually as soon as the sample holder temperature dropped to 250 °C. The sample was then withdrawn out of the vacuum system and investigated by SEM. The experimental conditions were:

- $T_a = 1100\,^\circ\mathrm{C}$
- $t_a = (30 - 60)\,\mathrm{min}$ (altered parameter)
- $T_1(\mathrm{In})/T_2(\mathrm{In}) = 770/870\,^\circ\mathrm{C}$

  (corresponding indium flux: $r(\mathrm{In}) = 5{,}3\,\mathrm{Å/min}$)
- $T_1(\mathrm{As})/T_2(\mathrm{As}) = 250/400\ ^\circ\mathrm{C}$
- $T_s = 600^\circ\mathrm{C}$
- $t_s = 45\,\mathrm{min}$
- $p = (2{,}0 - 2{,}5) \cdot 10^{-5}\,\mathrm{mbar}$

The annealing time was the altered parameter, which enables to control over the oxide decomposition process. In order to investigate the oxide layer decomposition before the InAs deposition, an atomic force microscopy (AFM) measurement was conducted. Samples were annealed at 1100 °C for 30, 45 and 60 min which corresponds with the annealing step used in actual growth experiments. The results are presented in figure 4.6. The shortest (30 min) annealing time did not create surface sufficiently modified for nanowire growth. 45 minutes long annealing seems to be optimal for creating pinholes in the oxide layer serving well for nanowires nucleation during the deposition. The longest (60 min) annealing time also resulted to creation of oxide openings.

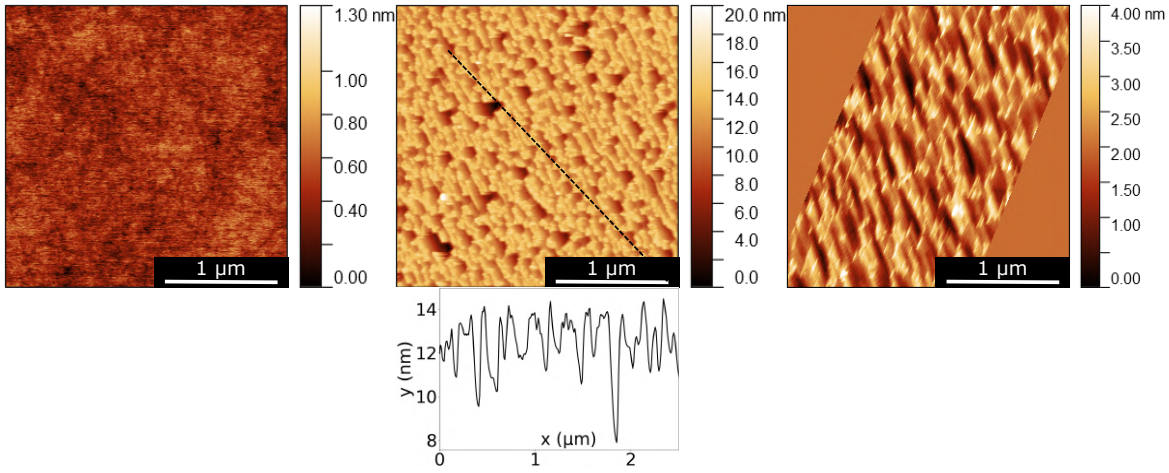
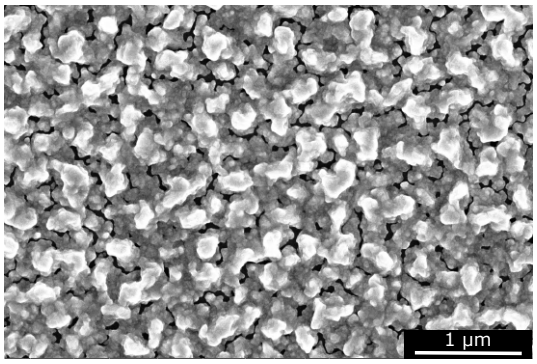
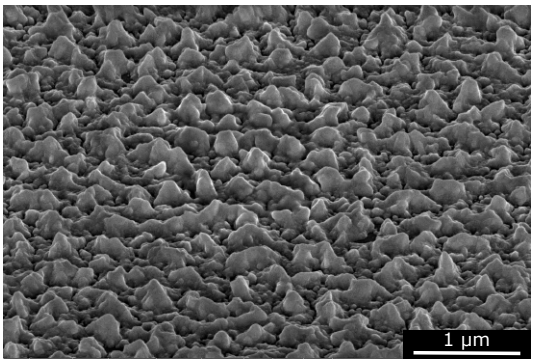


Figure 4.6: The surface topography of silicon substrate with native dioxide layer annealed at 1100 °C for 60 min (left), 45 min (middle) and 30 min (right). An AFM topography profile taken on the diagonal added for the middle image. The right image was post edited using thermal drift correction in Gwyddion software [64].

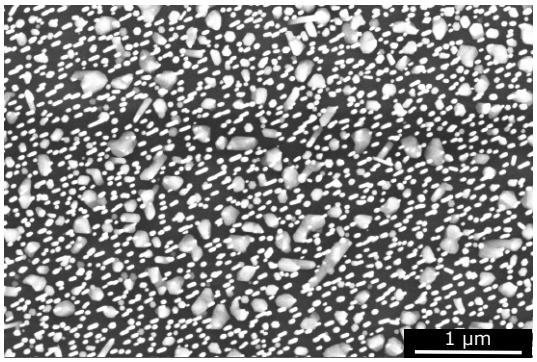
The deposition experiments were performed after investigating the relation between annealing time and substrate topography. The deposition parameters were identical for all cases, except for annealing time, as stated above. The images of grown InAs nanostructures are shown in figure 4.7.



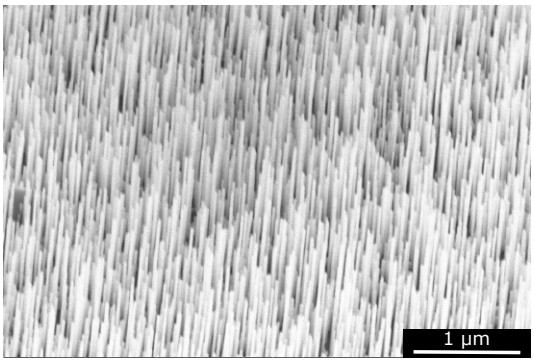
Sample A: top view
$t_a = 60\,\text{min}$



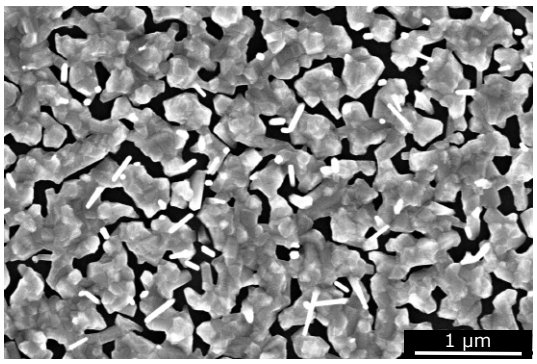
Sample A: 55° view
$t_a = 60\,\text{min}$



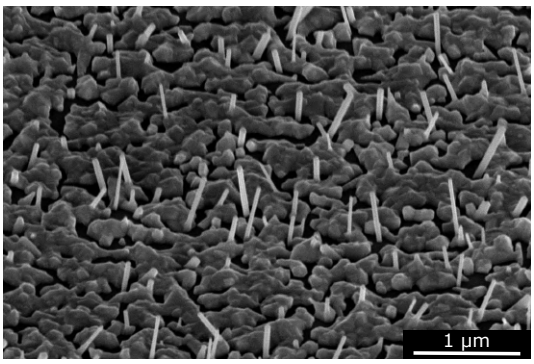
Sample B: top view
$t_a = 45\,\text{min}$



Sample B: 55°view
$t_a = 45\,\text{min}$



Sample C: top view
$t_a = 30\,\text{min}$



Sample C: 55°view
$t_a = 30\,\text{min}$

Figure 4.7: Selective area epitaxy InAs nanowires. Experimental series investigated annealing time ($t_a = 30, 45, 60\,\text{min}$) as an optimized parameter. Left column presents particular sample top view. Right column 55° tilted view. All images taken by SEM FEI Verios 460L.

The InAs growth mechanism corresponds considerably with the substrate topography after a correspondingly long annealing. On the sample A, there are no nanowires, only bulk InAs material in the form of layers and islands. The silicon dioxide layer was probably fully or almost fully thermally decomposed. This fact led to a large area of oxide uncovered silicon substrate where the epitaxial growth of the

deposited material is naturally higher. Because there were no larger oxide areas preventing the epitaxy, the deposition then resulted in a fully covered substrate. Under stated experimental conditions, a combined (layer and island) growth mechanism was then preferred.

The sample B annealed for 45 min became highly covered by InAs nanowire structures. The top view reveals that there is a small amount of parasitic bulk crystals on the surface between the nanowires. This phenomenon may originate, for example, from the presence of impurities on the substrate resulting from silicon cutting or insufficient cleaning. Such imperfections are then favored as nucleation sites. The nanowires growth direction is perpendicular to the surface in the direction $\langle 111 \rangle$, which is typical for nanowires prepared on silicon (111) substrates [65, 66, 67]. Small deviations from the $\langle 111 \rangle$ directions are limited to a few degrees at most. They can be associated to strain-induced effects [68]. InAs SAE nanowires exhibit dispersion over length and diameters. The nanowires dimensions vary from 20 nm to approximately 80 nm in diameter while their length reaches from hundreds of nanometers up to over one micrometer. The position of the nanowires is also random as typical for growth on thermally decomposed substrates.

On sample C, annealed for 30 min, there are a minimum of InAs nanowires visible in combination with considerable parasitic growth. The substrate surface is covered by an almost fully grown layer with a small amount of nanowires nucleated from bulk crystals. For this reason, the growth direction of nanowires is not $\langle 111 \rangle$ anymore as the nanowires growth direction is in most cases determined by the crystalographic orientation of InAs bulk material underneath. The nanowires reach maximum of several hundrets nanometers with the diameter up to approximately 80 nm.

4.4 Positional control of nanowires growth

For many potential applications of nanowires, it is highly advantageous to be able to precisely control their geometry (i.e., length, radius) and their exact position or mutual position in an array of nanowires [69, 70]. Fabrication of nanowires accurately located over a large area arrays is thus essential technological challenge. This idea requires highly controlled fabrication of preferential nucleation spots for the following growth. The most commonly used methods for substrate preparation for both VLS and SAE growth are patterning the substrate by focused ion beam (FIB) or electron beam lithography (EBL).

One of the goals of the diploma thesis was aimed at the preparation of InAs nanowires with high control over their position and developing a technological process for the fabrication of such a structures with sufficient level of repeatability. Since the preparation of self-seeded nanowires in the chamber turned out to be technologically demanding if not impossible as discussed in section 4.3, the work was focused on the fabrication of SAE InAs nanowires arrays.

4.4.1 Preparation of substrate

One of the most widely used approaches of positionally controlled nanowire growth is currently the combination of electron beam lithography and wet etching [71, 72] or reactive ion etching (RIE) [73, 74]. For the growth of InAs nanowires on a silicon substrate, which is also presented in this work, a patterned layer of silicon dioxide is usually used. Same approach was used in experiments presented in this thesis. As a first step of substrate modification, a layer of SiO_2 was formed on the silicon substrate. The silicon dioxide layer was prepared by atomic layer deposition (ALD) using tris dimethyl amino silane (TDMASi) as precursor. The deposition process was performed at a temperature of 200 °C using plasma enhanced mode. Continuous layer with thickness of 5,3 nm was formed during this process. Together with a native silicon dioxide covering the silicon wafer, the oxide thickness is 6,5 nm in total. The thickness was found experimentally by ellipsometric measurement.

Polymethylmetacrylate (PMMA) (product designation 649.04) was used as an electron beam resist. Samples were cleaned and annealed at 100 °C for 60 s to desorb organic residues. The resist was spin coated for 60 s on 4000 rpm. According to the resist manufacturer, such a process results in a resist thickness of 150 nm [75]. Afterwards, the spin-coated samples were post baked for 3 min at 150 °C. Electron lithography was performed on Scanning Electron Microscope/E-beam writer TESCAN MIRA3/Raith LIS instrument. The accelerating voltage was set to 30 kV and beam current was set to 150 pA. The pattern irradiated by the electron beam had the shape of a periodic array of circular holes. The individual holes were 1 µm apart and their radius was 200 nm. This value was chosen because it was the smallest dimension that was achieved using above mentioned resist. Klayout software was used for designing the patterns.

The developer recommended by the manufacturer was used after electron beam irradiation. The developing step lasted 3 min as recommended. The developing was stopped by dipping the samples into IPA. Samples were cleaned in distilled water and by pure nitrogen stream afterwards. The actual production of holes in the oxide layer was ensured by wet chemical etching using buffered hydrofluoric acid (BHF). The samples were dipped in for 2 seconds. The etching process was stopped by immersion of the substrate in distilled water. The PMMA resist layer was then stripped off in acetone ultrasonic bath. Manufactured patterned silicon substrates were stored inside IPA to prevent the reoxidation process at the bottom of the holes. Samples were taken out during the very last moment before loading into UHV system and cleaned by nitrogen gas. The above described technological process resulted in substrates with precisely defined holes in the silicon dioxide layer as shown in figure 4.8. Holes have diameter of approximately 280 nm and mutual distance of their centres are 1 micron in both axis. The larger diameter of the holes than the diameter in the Klayout design was caused by considerable underetching of the resist mask. Arrays of such a geometry were used for most of the experiments since the diameter was the smallest one, which was able to be fabricated using described process. The dimeter of holes could differ slightly for different substrate pieces as the short etching time could cause high relative error.

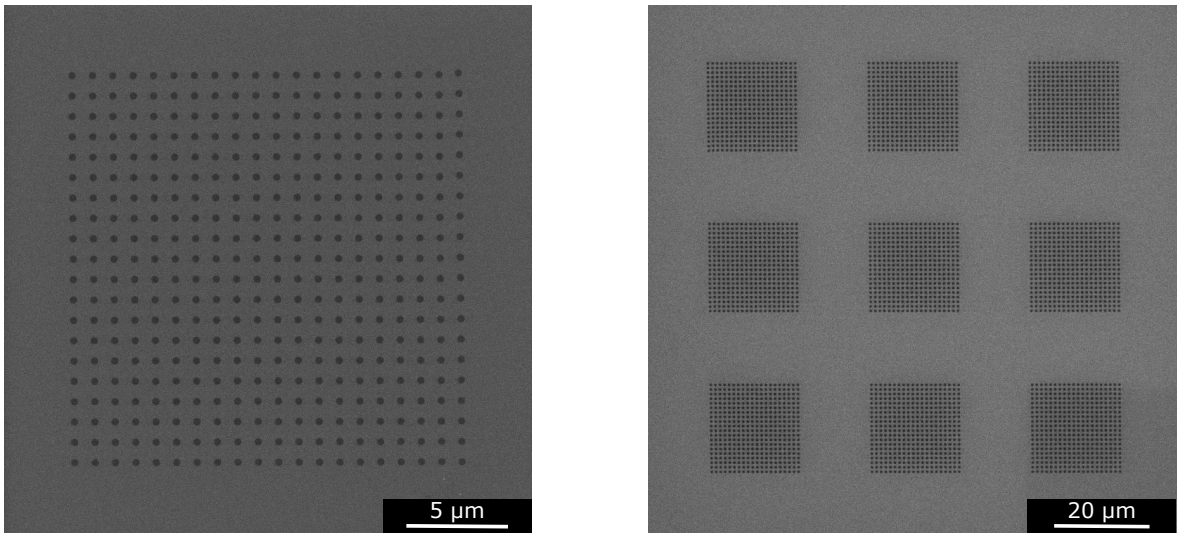


Figure 4.8: An array of holes in silicon oxide fabricated by the combination of electron beam lithography and wet chemical etching. The diameter of the hole is 280 nm. The mutual distance is 1 µm in both axis. Right image presents 3×3 matrix of arrays. The images were taken by TESCAN MIRA electron microscope.

4.4.2 Deposition

Similar deposition parameters as those presented in section 4.3 were used for deposition on lithographically patterned substrates. In comparison with depositions performed on bare substrate, the annealing procedure was now unnecessary since the lithographic etching should have provided the preferential nucleation centers on the substrate. Individual depositions were defined by following parameters:

- $T_1(\mathrm{In})/T_2(\mathrm{In}) = (710/810 - 770/870)\,^{\circ}\mathrm{C}$ (altered parameter)

  (corresponding indium flux: $r(\mathrm{In}) = (1{,}6 - 5{,}3\,\mathrm{\AA/min})$

- $T_1(\mathrm{As})/T_2(\mathrm{As}) = 250/400\ ^{\circ}\mathrm{C}$
- $T_\mathrm{s} = (600 - 630)^{\circ}\mathrm{C}$ (altered parameter)
- $t = 25\,\mathrm{min}$
- $p = (2{,}2 - 3{,}4) \cdot 10^{-5}\,\mathrm{mbar}$

All samples were investigated by SEM. The results are presented in figure 4.9. The SEM images show a clear dependence of crystallization and growth mechanism of InAs nanowires on substrate temperature and on the indium flux. For set of higher temperatures the desorption of atoms is significantly predominant resulting in creating smaller structures. The crystals are obviously bigger for depositions performed with higher fluxes. The diffusion length of atoms on the surface increases with increasing substrate temperature. Atoms from surrounding with bigger radius can therefore diffuse into the oxide mask opening. On the other hand, as the temperature increases, the probability of desorption increases. Higher diffusion length also increases the number of atoms which can contribute to the formation of nanowires by diffusion along its walls. In experiments, it is therefore necessary to find a balance between these two opposing phenomena to find ideal set of parameters.

A positionally controlled array of InAs nanowires is visible on the sample A. This could be also seen in the larger field of view image 4.10. The combination of experimental parameters resulted in the formation of nanowires with remarkably uniform dimensions. The nanowires length reaches up to more than one micrometer and the typical diameter is around 50 nm. Multiple nanowires were formed within one mask opening. This phenomenon has been reported for InAs nanowires grown in SiO_2 masked Si substrate [39] and is beeing associated with the oxide opening size. The growth direction usually corresponds with $\langle 111 \rangle$, nanowires, thus in most of the cases growth perpendicular to the substrate surface. However, many 1D structures do not follow this trend. This phenomenon is most likely caused by the amount of bulk crystals nearby the nanowires. Crystal facets of bulk structures can then influence the growth direction. Nanowires growing from bulk InAs material are also observable. It is not clear whether the hole is first filled with bulk InAs followed by the formation of nanowires or whether the process is reversed. Both mechanisms can also occur simultaneously. An in-situ technique would be necessary for investigating this process.

Another possibility would be performing of several identical depositions lasting different time. This experiment would however be extremely time consuming and could thus not be performed due to time constraints. The space in between the etched openings is almost uncovered by any material.

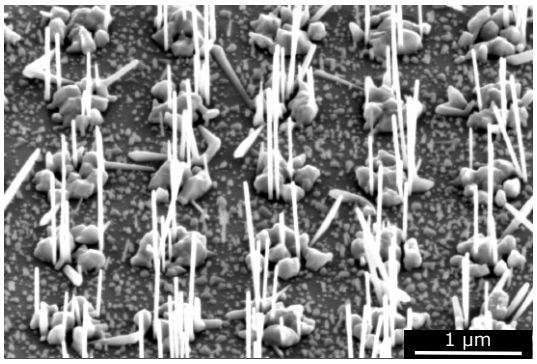
The deposition on sample B resulted in positionally controlled crystal growth. However, one dimensional structures are only occasionally formed in predefined spots. Their length reaches only few tens of nanometers. The vast majority of etch-modified openings are filled only by bulk InAs crystals. In addition, the remaining substrate surface is uniformly covered with smaller InAs islands.

Several whiskers are visible on the sample C. Their length reaches from hundreds of nanometers to approximately one micrometer. Their growth direction is nevertheless in some cases random or they do not even nucleate from any of the defined holes. The etched oxide openings are filled by bulk InAs and the whole surface is covered by fully formed InAs layer.

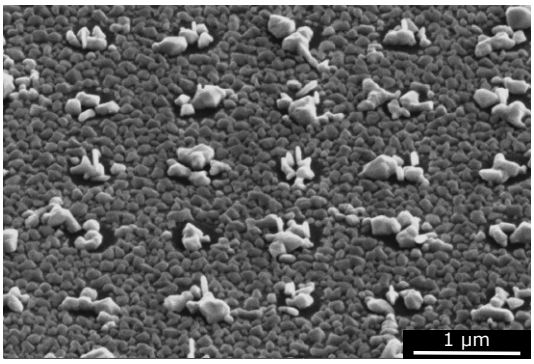
No interesting structures can be seen in the image D. Desorption was probably highly predominant phenomenon in this case. This is also the reason that the deposition which logically follows (potential sample F) was not executed because is reasonable to assume that the same temperature combined with even lower indium flux would not bring any new results.

Structures created on the sample E are considerably nonuniform. It can be clearly stated that substrate openings serve as preferential spots for nucleation. Formation of two, three or even more nuclei is visible. The nucleation point seems to be close to the edge of mask opening in most cases. Similar behaviour was reported in [67]. Crystals formed in the middle of opening are nevertheless also reported. Nanowires grew from several holes. Their length and diameter vary significantly. InAs crystals in the form of bulk or 1D shapes were formed also on the surface outside the openings. However, the surface of the oxide layer remained mostly uncovered.

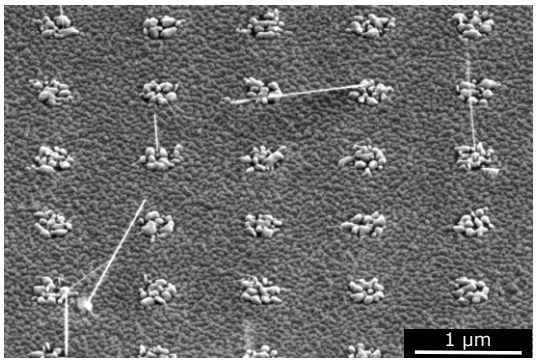
Unexpected formation of very compact layers on the samples B and C led to considerations about the quality of SiO_2 layer. It is notable from the sample E that the SiO_2 is definitelly not atomically smooth as expected. The question rises whether the oxide is actually present on samples B and C as epitaxial growth at oxide-coated sites should be highly non-preferred. The SiO_2 thickness plays a dominant role for InAs epitaxy mechanism according to [76]. A possible explanation for such behavior is too high growth temperature, which could possibly cause thermal decomposition of SiO_2. Another question arising from the results of the deposition is whether there is really bare silicon at the bottom of the holes or SiO_2. The presence of slight amount of silicon oxide at the bottom of the holes would explain unexpected nonuniformity of the sample E. For these reasons, further research was focused on a detailed understanding of the properties of oxide patterned substrates. The experiments investigating the influence deposition process on substrate quality are presented in following section 4.4.3.



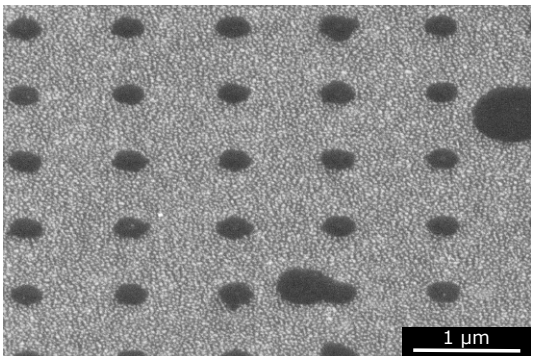
Sample A:
$T_s = 600\,°C$
$T_1(\mathrm{In})/T_2(\mathrm{In}) = 770/870\,°C$
$r(\mathrm{In}) = 5{,}3\,Å/\mathrm{min}$



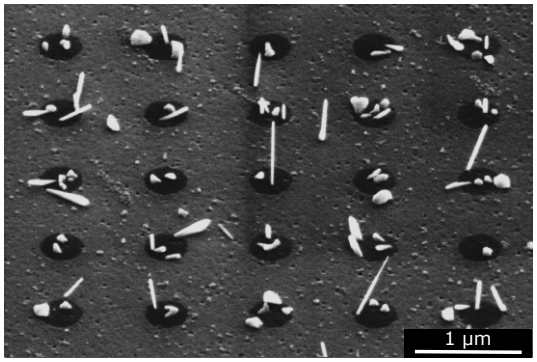
Sample B:
$T_s = 630\,°C$
$T_1(\mathrm{In})/T_2(\mathrm{In}) = 770/870\,°C$
$r(\mathrm{In}) = 5{,}3\,Å/\mathrm{min}$



Sample C:
$T_s = 600\,°C$
$T_1(\mathrm{In})/T_2(\mathrm{In}) = 740/840\,°C$
$r(\mathrm{In}) = 2{,}9\,Å/\mathrm{min}$



Sample D:
$T_s = 630\,°C$
$T_1(\mathrm{In})/T_2(\mathrm{In}) = 740/840\,°C$
$r(\mathrm{In}) = 2{,}9\,Å/\mathrm{min}$



Sample E:
$T_s = 600\,°C$
$T_1(\mathrm{In})/T_2(\mathrm{In}) = 710/810\,°C$
$r(\mathrm{In}) = 1{,}6\,Å/\mathrm{min}$

Figure 4.9: The result of deposition in lithographically patterned substrates. Individual samples differ in substrate temperature $T_s = (600 - 630)°C$ and indium flux $r(\mathrm{In}) = (1{,}6 - 5{,}3)\,Å/\mathrm{min}$. Remaining parameters were kept identical for all cases. $t_s = 25\,\mathrm{min}$, $T_1(\mathrm{As})/T_2(\mathrm{As}) = 250/400$ °C. All images taken by SEM FEI Verios 460L under 50° tilt.

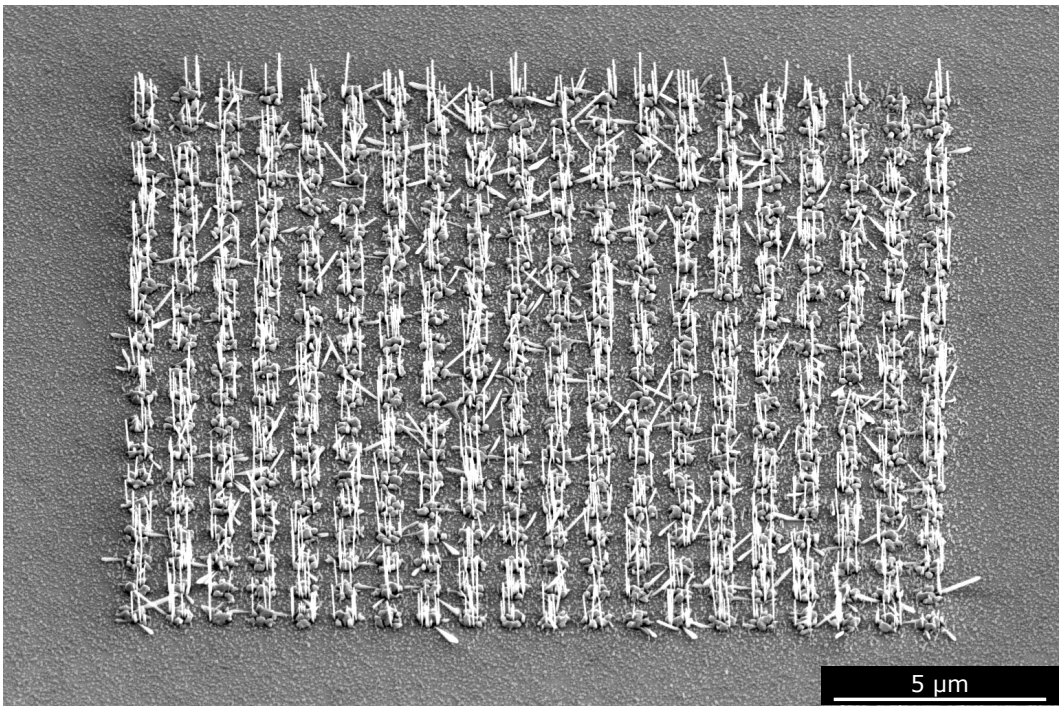


Figure 4.10: Sample A: 50° tilted view on array consisting of 20 times 20 holes.

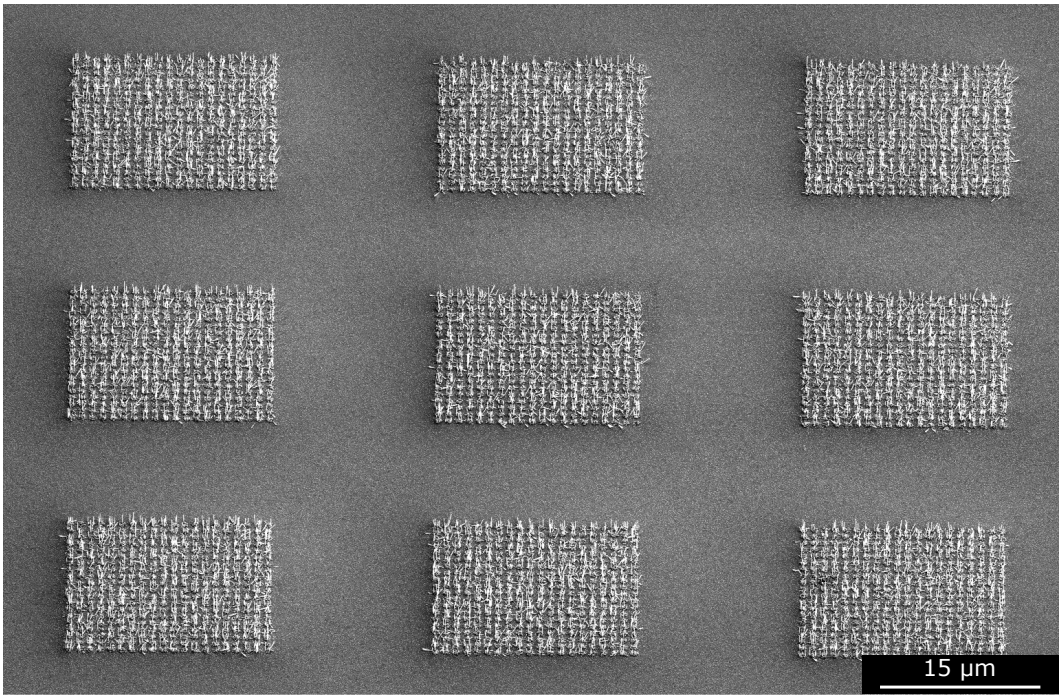


Figure 4.11: Sample A: 50° tilted view on matrix consisting of 3×3 arrays.

4.4.3 Investigation of substrate quality

The effect of substrate temperature during deposition on silicon dioxide quality was investigated using AFM and ellipsometry. First, a measurement of the SiO_2 thickness after BHF etching dip was done. The goal was to detect possible presence of SiO_2 in the bottom of the oxide mask opening after etching. A piece of silicon substrate with 6,5 nm thick SiO_2 was dipped for 2 s in BHF. Afterwards, the thickness of the remaining oxide layer was measured using ellipsometry. The measurement showed that there is aproximately 1,8 nm oxide remaining after the 2s etching step.

An AFM measurement was also performed on the patterned substrate. SPM Bruker Dimension ICON instrument in peak-force tapping mode was used for this purpose. The topography measurements confirmed the cylindrical shape of the etched holes. The diameter of the presented holes is 270 nm and their depth is about 4.5 nm. This confirmed that the etching step is the least repeatable step in the whole fabrication process. The diameters of the holes on the individual samples can vary in the order of tens of nanometers. Their depth can then vary up to approximately one nanometer. The solution for better repeatability could be to use a weaker etching mixture. A longer etching time would then reduce the relative time error. The detail of the oxide mask opening shows that its bottom is not absolutely flat. It can have an impact on the nucleation mechanism. The AFM image also reveals the presence of resist residues on the substrate surface outside the oxide opening. Excessive amount of resist could explain the unexpected growth on the surface in unpatterned areas, since this residual contamination decreases the diffusion length and acts as a nucleation spot.

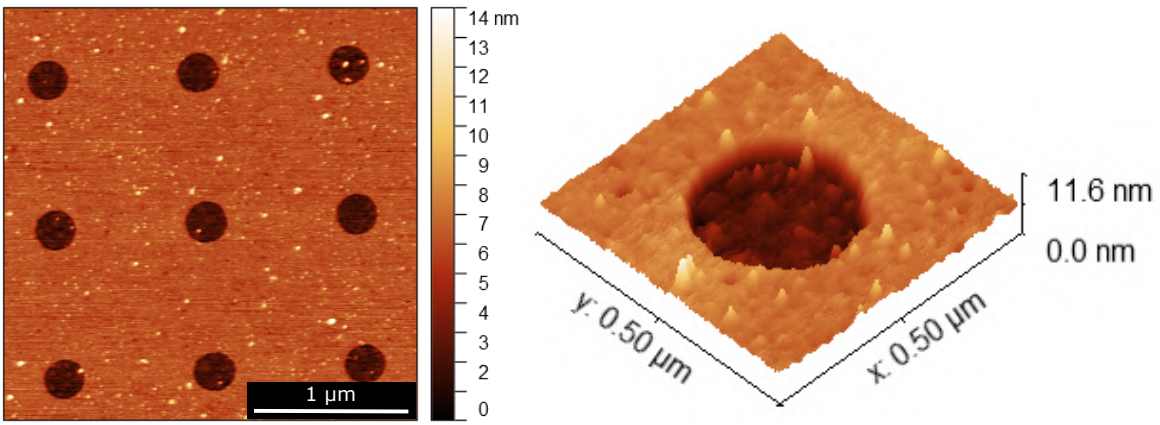


Figure 4.12: Topography image of an 3 × 3 holes part of the array (left). A detailed view of one hole topography (right).

The possibility of SiO_2 layer thermal decomposition during the growth process was also investigated. The substrate with the standard oxide layer used in the experiments was heated identically to the used deposition processes inside MBE chamber. The SiO_2 thickness was measured afterwards using ellipsometry. The results are presented in the table 4.4.3. The topography was measured afterwards to determine any change in surface roughness. The root mean square roughness value was also added to the table. The AFM measurements results are presented in figure 4.13.

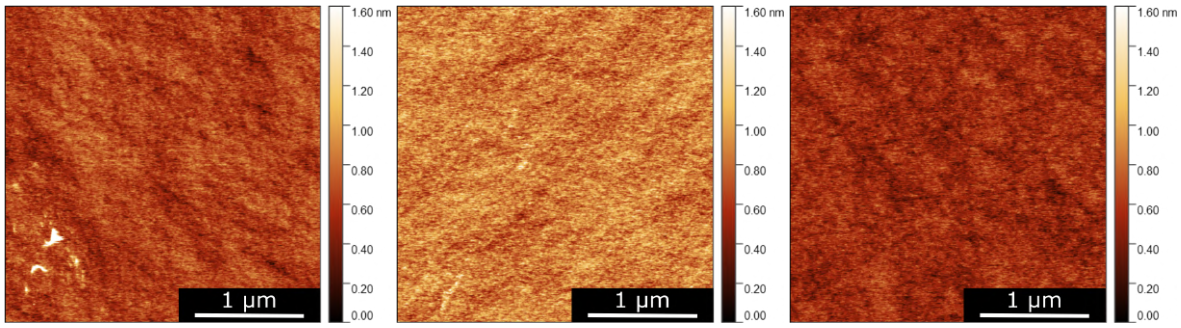


Figure 4.13: Surface topography of the substrate before growth process (left), the sample annealed at 600 °C for 25 min (middle), the sample annealed at 630 °C for 25 min.

	SiO_2 thickness	RMS roughness
before the growth process	$(6{,}50 \pm 0{,}03)$ nm	(128 ± 5) pm
after the growth process (600 °C for 25 min)	$(6{,}00 \pm 0{,}03)$ nm	(158 ± 4) pm
after the growth process (630 °C for 25 min)	$(6{,}00 \pm 0{,}03)$ nm	(121 ± 2) pm

The measurement thus suggests that the thickness of the oxide layer may decrease due to the temperature during deposition. However, the roughness of the sample is apparently not significantly modified. Therefore, this phenomenon may affect the growth mechanism, but it could not be considered dominant and can not fully explain the layer growth behaviour discussed in section 4.4.2. The cause of the uniform layers formation outside the silicon dioxide mask openings in some depositions thus remains unclear, however, it is most likely not caused by the change in layer properties caused by deposition temperature. A possible explanation may be related for example with the presence of an increased amount of resist residue on the surface which would increase the probability of crystallization. This presumption would have to be, however, further investigated.

5 CONCLUSION

The theoretical part of the diploma thesis presents a brief introduction into III-V semiconductors. It summarizes their basic properties, potential applications, and the motivation for their research. Special attention is paid to indium arsenide (InAs) as the material investigated in the experimental part of the work. The text continues with the description of two basic mechanisms for nanowire growth, namely, the selective area epitaxy (SAE) mechanism and the vapour-liquid-solid (VLS) mechanism. The second chapter lists the most important experimental techniques used in the practical part of the work, namely, molecular beam epitaxy (MBE), scanning electron microscopy (SEM), and electron beam lithography (EBL).

The main content of the experimental part was the preparation of InAs nanowires by multiple approaches. The aim was to find deposition conditions for the growth of InAs nanowires with sufficient quality and reproducibility, enabling further study of such 1D structures. Nanowires were fabricated using the molecular beam epitaxy method (MBE) and were prepared on native silicon substrate resulting in high area coverage growth and silicon dioxide patterned substrate enabling control over the nanowires growth position. First, the experiments focused on the preparation of indium catalysts in the form of droplets for the growth of self-seeded nanowires via VLS are discussed. The experiments have shown that the preparation of self-seeded InAs nanowires in the particular MBE chamber is very technologically demanding and the possibility of production of indium self-catalyzed nanowires via VLS mechanism is not possible in the standard configuration due to high stable arsenic partial pressure.

The work was therefore focused on the fabrication of nanowires via the SAE mechanism. The thermal annealing of silicon dioxide native layer was used for substrate modification suitable for nanowire growth. The annealing procedure was optimized which resulted in high coverage of InAs nanowires growth on silicon. Obtained nanowires have a diameter between (20-80) nm. Their lengths reach from hundreds of nanometers up to over one micrometer. The nanowires growth in $\langle 111 \rangle$ direction as typical for nanowires grown on Si(111) substrate [66, 67].

The second approach aimed at positionally controlled nanowires growth. The combination of atomic layer deposition (ALD), electron beam lithography, and wet chemical etching was used for modification of the substrate suitable for positionally controlled growth. It consists of etching with buffered hydrofluoric acid (BHF) through a PMMA lithographic mask leading to the production of circular openings in the silicon dioxide layer. The effect of growth temperature and indium flux was investigated on such modified substrates. The combination of growth temperature

and indium flux (600°C and 5,3 Å/min, respectively) led to the best results and positionally controlled nanowires growth. The experiments show that the nanowires tend to nucleate at the edge of the silicon dioxide mask opening. Fabricated nanowires have relatively uniform dimensions. The length reaches up to one micrometer and the diameter is approximately 50 nm. Using the mentioned parameters, it was possible to achieve hundred percent yield of mask opening for growth, although individual mask openings are always used for nucleation of multiple nanowires. This phenomenon is in accordance with the literature and is related to the mask opening size [39]. The substrate preparation process for the production of mask openings with smaller diameters has to be further optimized for the growth of only one nanowire from an individual opening. The results of this thesis are, nevertheless, the first step towards positionally controlled growth of nanowires at Institute of Physical Engineering. The influence of the growth temperature on the substrate quality and the growth mechanism is briefly discussed at the end of the work.

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